Optimized Charge Pump with Clock Booster for Reduced Rise Time or Silicon Area

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Nowadays, Charge Pumps (CPs) are essential building blocks which are finding a wide application in several microelectronic circuits and embedded systems. This not only for the strongly increase in the μ-processor and non-volatile memory market, where they are almost always present, but also for their inclusion on energy harvesting systems, smart sensors and the emerging Internet-of-Things (IoT) devices. In all these applications, improvement of speed performance and area occupation represent key design parameters whose optimization requires new design strategies and modelling. Among the various strategies, Clock Boosting is a promising technique that, through clock signal amplified by a booster (CKB), allows reducing the necessary number of stages, N, to get the nominal output voltage. Being the pump-up time and the occupied silicon area strongly dependent on N, they could also be significantly reduced [1]-[3]. In real applications, however, the potential speed advantage is limited by driving capability of the CKB, hence, a sizing strategy to obviate this drawback is investigated. With this in mind, the presented work proposes two design methods to size Dual-Branch Cross-coupled CPs with boosted clock signals (Fig. 1), both with the aim of optimizing speed performance or area occupation [4].

By careful analysis of the circuit depicted in Fig.1, the pump-up time depends on how the capacitance of the entire system, C_{DCP}, is parted between the sum of the pumping capacitances and the clock booster's capacitance. The result is the possibility to adopt an optimum distribution way, function of C_L/C_{DCP}, in order to reduce settling time for equal area occupation ($\alpha_{T,opt}$) or, vice-versa, to reduce silicon occupied area ($\alpha_{A,opt}$) for equal settling time:

$$\alpha_{r,opt} = 3\frac{C_L}{C_T}\left(\sqrt{1+\frac{1}{3\frac{C_L}{C_T}}}-1\right), \quad \alpha_{A,opt} = \frac{1}{2} - \frac{1}{8\left(1+3\frac{C_L}{C_{DCP}}\right)} \quad (1)$$

Their distributions are reported in the graphs of Fig.2. To verify the advantages of the proposed strategies, the new topology has been compared to the traditional Dual-Branch Cross-Coupled CP in terms of area occupation (Fig.3) and both have been simulated with different number of stages and various output capacitance values in SPICE environment, with ideal devices and in 65-nm CMOS technology. Their normalized rise time have been reported in the graphs of Fig.4, proving that the proposed methods allow to improve CP's performance mainly for load lower than total capacitance of the system.

References

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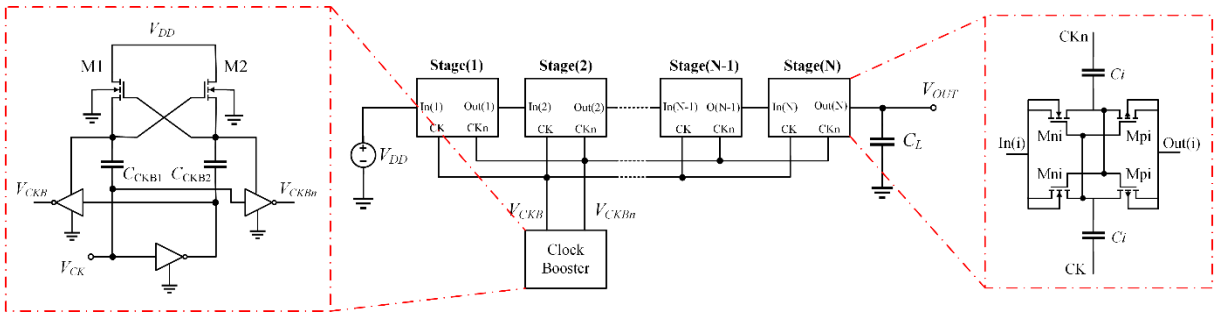

Figure 1: Schematic of the Dual-Branch Cross-Coupled charge pump and the clock booster.

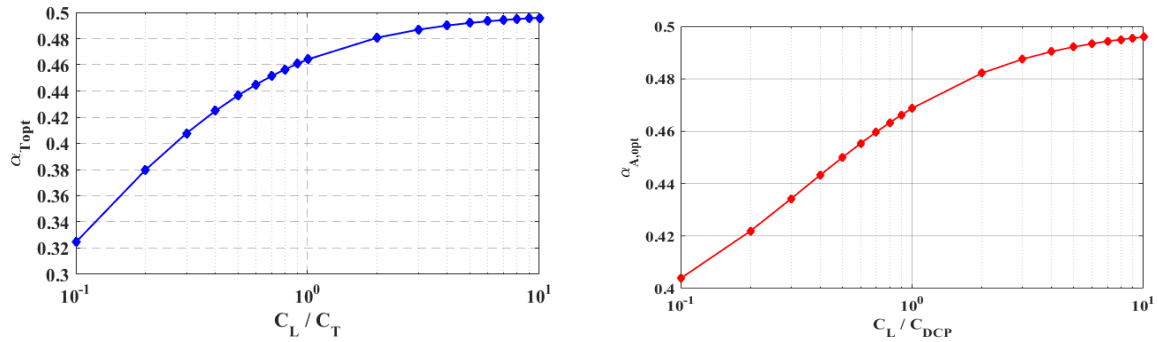

Figure 2: Optimum values of the scaling factor α versus C_L/C_{DCP} for reduction of: (a) rise time (left); (b) silicon area (right).

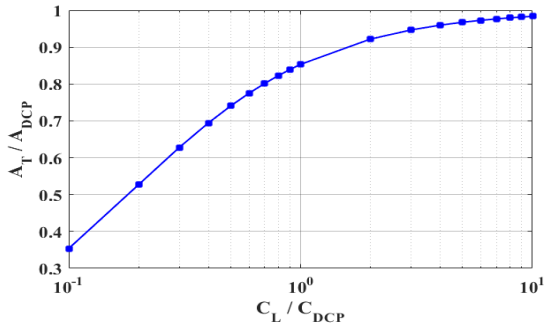

Figure 3: Silicon area reduction as a of function of C_L/C_{DCP} under optimum design condition.

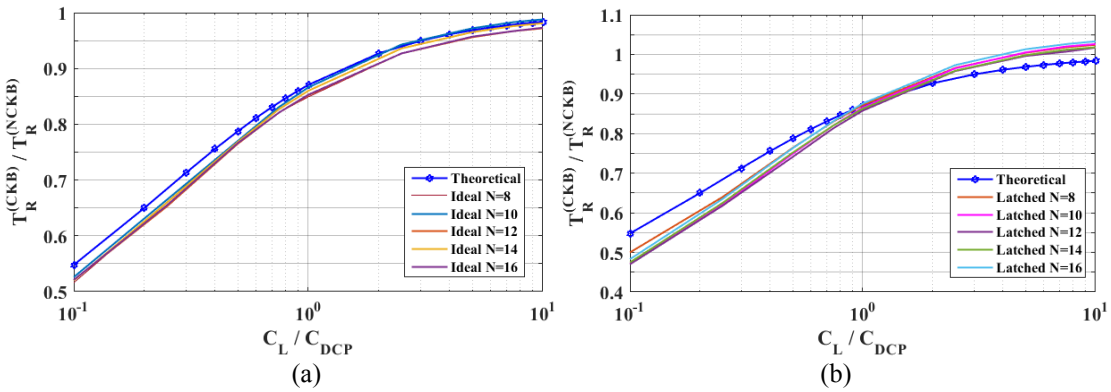

Figure 4: Simulated rise time ratio versus C_L/C_{DCP} using: (a) ideal switches; (b) and transistor-level implementation.