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Exploring Electrical and Thermal Properties of Surrounding Gate FETs and FinFET Transistors: Insights from Simulation and Experimentation

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***Abstract*—Surrounding Gate FETs and FinFET transistors are interesting options for semiconductor technology, and this study looks into their electrical and thermal properties. We have produced encouraging simulation findings that agree well with both experimental and numerical data, using an electrothermal model that integrates the new Stephan-Boltzmann model, the enhanced Ballistic-Diffusive model, and the enhanced Drift-Diffusion model. Further examination of the Surrounding Gate FET indicates the appearance of phonon radiation effects when the channel length is reduced to 10 nm.**

***Index Terms*—FET Surrounding Gate, FinFET transistors, electrical and thermal behavior, electrothermal model, phonon radiation effect.**

I. Introduction

For low-power applications, complementary metal-oxide semiconductor (CMOS) circuits have become the technology of choice [1]. According to forecasts made by the International Roadmap for Devices and Systems (IRDS) [2], CMOS technology will have reached its limit since its birth in 1963 [3]. This is projected to happen by 2034. Alternative architectural approaches have the potential to maintain Moore's law in light of the approaching end of metal-oxide semiconductor field-effect transistor (MOSFET) technology [4]. Fin Field-Effect Transistors (FinFETs) have been identified as promising prospects among these, with progress in the semiconductor industry slowing down at the 10-nm node [5].

Nevertheless, additional scaling presents a number of technical difficulties that need to be resolved [6], [8], [13]. It is necessary to lower the heat generation rate in comparison to MOSFET transistors. Thinner fins must be used to provide good electrostatics, however this can reduce carrier mobility relative to MOSFET devices and result in large threshold voltage changes. In parallel, Surrounding Gate (SG) FET transistors have been implemented to improve electrostatics and channel widths while reducing the impacts of small channels [9], [11], [12], [14]. Moreover, by adjusting the surrounding gate widths, SG FET transistors can be vertically integrated to save space in integrated circuits and modify the transfer characteristics [12].

The electrical performance of FinFETs and SG FETs has been extensively studied [13]–[15]. Nevertheless, only a small number of research works have created models to forecast heat transfer and phonon transport in nano FET devices [16]–[18]. Finding the highest working temperature that doesn't negatively impact the transistors' electrical responsiveness is the main goal of phonon transport in FinFETs and SG FETs.

Thus, the Finite Element Method was used to computationally investigate the electrothermal performances of the FinFETs and SG FETs. After FinFET and SG FET structural investigations, a mathematical method based on an electrothermal model was introduced. Furthermore, based on experimental and numerical studies, the transfer and output properties of FinFETs and SG FETs with various channel lengths were examined and verified [19]–[21].

II. Mathematical Model

To account for electron transport in the quasi-ballistic regime, the drift-diffusion model must be adjusted. In the macro/microscale domain, electron mobility remains constant, and this is essentially how the alteration is accomplished. In our instance, we created a model of effective electron mobility that is dependent on the electric field and gate bias. [24] provides the effective electron mobility model.

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_0}\left(\frac{1}{\theta_1\left(V_{gs}-V_{th}\right)} + \frac{1}{\theta_2\left(V_{gs}-V_{th}\right)^2}\right) \quad (1)$$

where θ_1 and θ_2 are fitting parameters that represent the mobility degradation owing to surface roughness scattering and phonon scattering, respectively, and μ_0 is the low field effective mobility.

An effective electron mobility model was implemented in the D-D model. The calibrated D-D model given by the

Poisson equation and the electron and hole equations is as follows:

$$\nabla(\varepsilon \nabla V) = -q(p - n + N_D - N_A) \tag{2}$$

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla(-qn\mu_{eff}\nabla V) - (R - G) \tag{3}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla(-qp\mu_{p}\nabla V) - (R - G) \tag{4}$$

where ε is the electrical permittivity, V is the electrical potential, q is the elementary charge, n and p are the electron and hole concentrations, respectively, N_D and N_A are the donor and acceptor concentrations, respectively, and (R-G) represents the generation recombination rate.

It becomes difficult to anticipate the heat conduction inside the nanotransistors due to this complicated heat transfer problem. The Joule effect and ballistic transport of phonons in the channel region of FET devices control the process of heat conduction. The following is how these two source terms are expressed:

$$Q = J.E + (R - G).(E_g + 3K_BT) \tag{5}$$

The electric field and current density, which are concentrated inside and on the borders of the channel region, are the primary factors that determine the Joule effect.

The heat transfer regime becomes quasi-ballistic when the mean free path exceeds the characteristic length. The local heat flux is assumed to be radiative and is defined as [25]:

$$q_b = \sigma T^2 \tag{6}$$

where σ is the Stephan–Boltzmann constant.

The classical ballistic-diffusive equation (BDE) could be written as follows [1]:

$$\tau_R \frac{\partial^2 T_m(r,t)}{\partial t^2} + \frac{\partial T_m(r,t)}{\partial t} = \frac{k_{eff}}{C}\nabla\nabla T_m(r,t) - \frac{1}{C}\nabla q_b(r,t) + \frac{Q}{C} + \frac{\tau_R}{C}\frac{\partial Q}{\partial t} \tag{7}$$

Combining equations (5 and 6) in Eq. 7, we obtain the new enhanced BDE model can be rewritten as follows:

$$\tau_R \frac{\partial^2 T(r,t)}{\partial t^2} + \frac{\partial T(r,t)}{\partial t} = \frac{k_{eff}}{C}\Delta T(r,t) - \frac{1}{C}\sigma.\nabla T^2 + \frac{(J.E+(R-G).(E_g+3K_BT)}{C} \tag{8}$$

The is the effective thermal conductivity k_{eff} is given as follows:

$$k_{eff}(Kn) = k\left[1 - \frac{2Kn \times \tanh(1/2Kn)}{1 + C_B \times \tanh(1/2Kn)}\right] \tag{9}$$

where τ_R is the relaxation time due to resistive collisions, C is volumetric heat capacity, $Kn = \frac{\Lambda}{L}$ is the Knudsen number, Λ is the phonon mean free path and L is the channel length of the proposed transistors, and C_B is constant which depends on the specularity parameter [26].

III. Structure to Model

In this study the devices that have been investigated are two state of the art transistors (FinFETs and SG FETs). The given electro-thermal investigation is based on numerical and experimental data's [19]–[21]. The main dimensions and doping values can be seen in Table I. The two schematic view of the studied devices are shown in Figure 1.

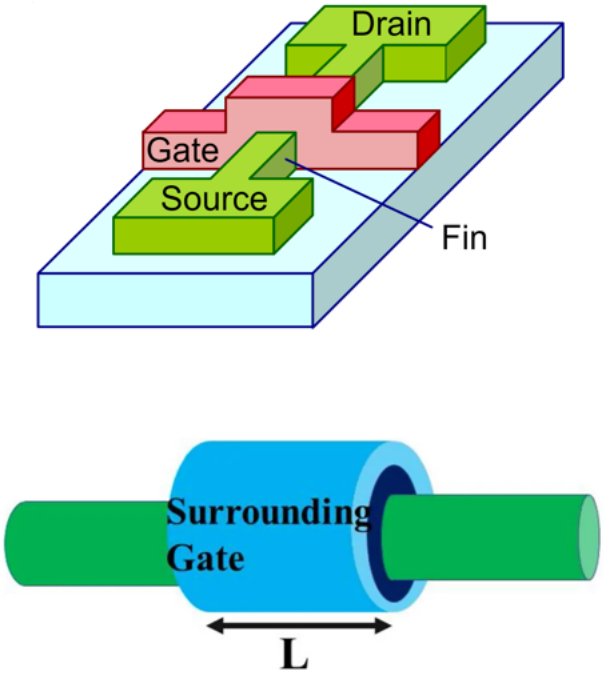

Fig. 1. schematic structure of SGT and FinFETs structure [22].

A schematic depiction of the FinFET investigated structures and the SGT transistor is presented in Figure 1. Here, we shall contrast experimental and numerical data with the transfer and output characteristics of the two specified architectures (with varying channel lengths). Additionally, we will look into how the temperature distribution inside the devices under study is affected by the channel length.

For foundry operations at 10 nm, 16 nm, and 50 nm, several channel lengths have been published; nonetheless, these numbers are considered as example. Different semiconductor foundries use different methods to quantify gate length in different nodes.

A gate length of 15 nm, for example, was published by IBM at Node 7 [23]. At the same node, TSMC claimed an effective gate length of 15 nm, hence our gate length is less than 15 nm. Initially, we looked into gate lengths of 10 nm, 16 nm, and 50 nm for various topologies in this study. Following the electrical model's validation, we looked at how gate length affected the thermal response of FinFET and SG-FET.

TABLE I
MAIN PARAMETERS USED IN OUR SIMULATION

	FinFET	SGFET
$L_g(nm)$	10	10
$H_{Fin}(nm)$	24	24
$W_{Fin}(nm)$	6.5	10
$EOT(nm)$	0.78	0.78
$N_{sub}(cm^{-3})$	1×10^{17}	1×10^{17}
$N_{subFin}(cm^{-3})$	5×10^{18}	5×10^{18}
$N_{Fin}(cm^{-3})$	1×10^{15}	1×10^{15}
$N_{S/D}(cm^{-3})$	2×10^{20}	2×10^{20}
$S/D(nm/dec)$	1	1

RESULTS AND DISCUSSIONS

A numerical simulation was conducted to verify the validity of the proposed electrical model. The devices used in the electrical simulation were a 50 nm SG FET and a FinFET device with channel lengths of 50 nm.

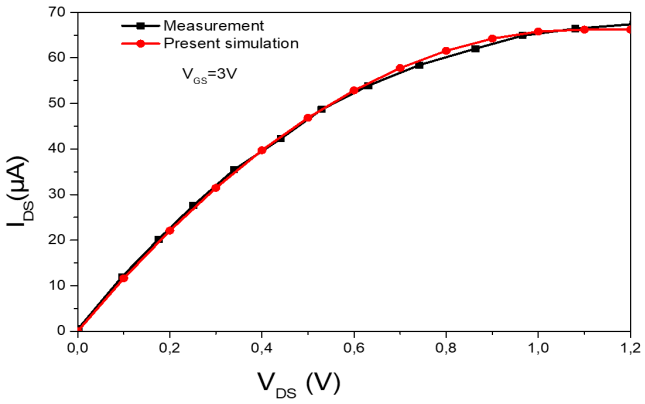

Fig. 2. Output characteristics comparison of SGT device with measured data [21].

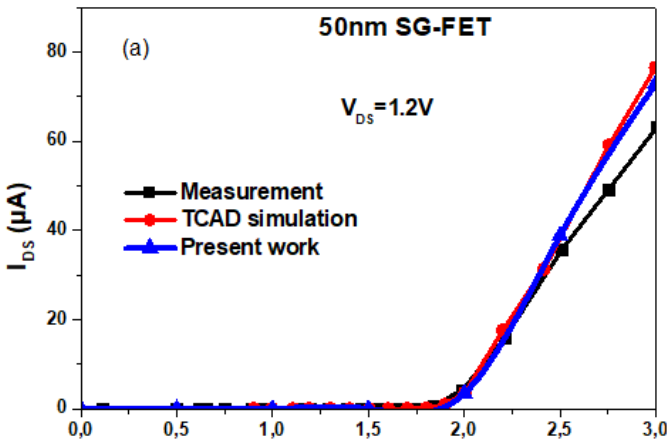

Fig. 3. Transfer characteristics comparison with measurement and TCAD simulation of 50 nm SGT transistor

The drain current–drain voltage of the surrounding gate transistor, as provided by our suggested electrical model, is compared with actual data at V_{GS}=3V from [21] in Figure 2. The model calculations (red line) and the experimental results (black line), as depicted in the image, agreed well.

The I_{DS}–V_{GS} characteristics of the 50 nm Surrounding Gate FET at V_{DS}=1.2V are displayed in Figure 3. The suggested model is in agreement with TCAD simulation [20], as illustrated in this figure.

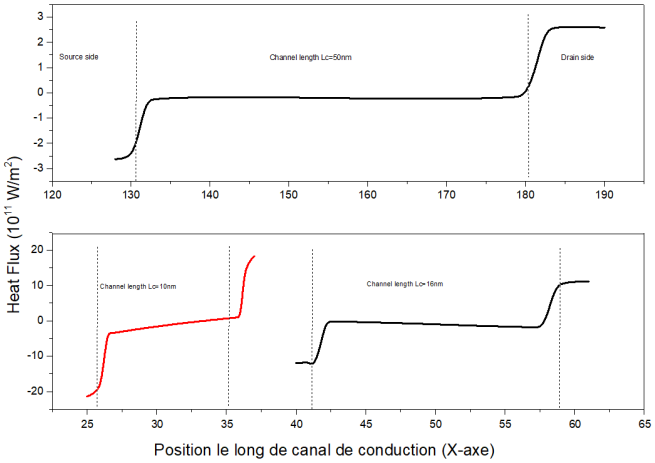

Fig. 4. Comparison heat flux along the channel region of the SGT device at t=50ns and V_{DS}=V_{GS}=1V with different channel region.

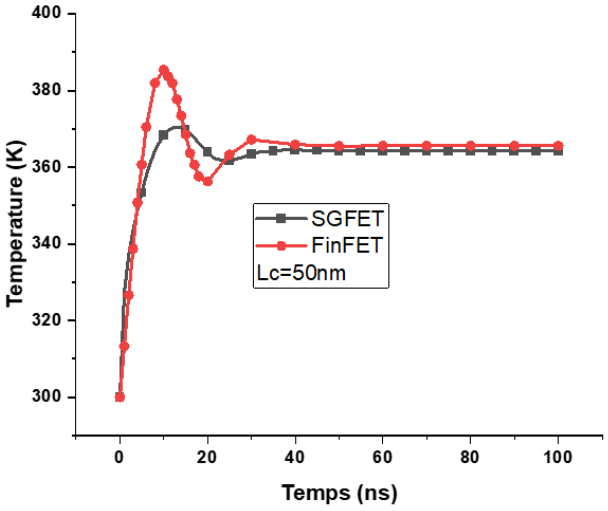

Fig. 5. Comparison of SG FET temperature at t = 50ns for LC=50nm and V_{DS}=V_{GS}=1V, depicting the evolution within the channel region of the SG FET and FinFET at V_{DS}=V_{GS}=1V.

In a comparative analysis of heat flux along the channel region of the SGT device at t=50ns and V_{DS}=V_{GS}=1V with varying channel lengths, it becomes evident from a thermal standpoint that the SGT transistor demonstrates pronounced temperature and heat flux distributions particularly when the channel length is 10 nm, as opposed to L_C=16 and 50 nm (see Figure 4).

Figure 5 provides a comparison of the temperature in SG FETs at t = 50ns for a channel length LC = 50 nm, with VDS=VGS=1V.

The data in the figure indicates that the temperature increases as the channel length decreases. Furthermore, we observed temperature variations from 0 to 35ns. This observation confirms that the temporal response of electron transport decreases with an increase in channel length.

CONCLUSION

Using a novel mathematical approach, this work reports on the electrical and thermal performance of FinFETs and surrounding gate FET devices with varying channel lengths. The outcomes achieved with the suggested electrical model are in good agreement with other simulation findings as well as experimental data. We connected the new Stefan–Boltzmann model with an improved D-D model and the BDE model for the first time. When considering the S-G transistor from a thermal perspective, we can say that, in contrast to L_C=16 and 50 nm, it has a significant temperature and heat flux distribution at a channel length of 10 nm.

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