EasyChair Preprint

№ 544

Exhaustive DFM Evaluation of Logic Cell Libraries via Virtual Characterization

Mehmet Meric Isgenc, Mayler Martins, Samuel Pagliarini and Larry Pileggi

September 29, 2018

Exhaustive DFM Evaluation of Logic Cell Libraries via Virtual Characterization

Meric Isgenc meric@cmu.edu
Mayler Martins mayler@cmu.edu
Samuel Pagliarini pagliarini@cmu.edu
Larry Pileggi pileggi@andrew.cmu.edu

ABSTRACT

Local layout effects create pattern dependencies at the 14nm node and below that make prediction of functional and parametric yield challenging. Because of exponential complexity of cell neighboring scenarios, pre-characterization of all patterns is impractical and silicon characterization is practically impossible. In this paper we propose a virtual characterization vehicle (VCV) methodology that can exhaustively identify all unique layout patterns as a function of a specified radius of influence. By exhaustively searching for patterns, these VCVs compile pattern frequency and expose hotspot patterns for all possible cell combinations. VCV results can guide the design and selection of logic cells in a library based on their impact on DFM metrics. Most importantly, these results can be used in silicon characterization vehicles to cover all possible layout patterns. Our VCV results show how DFM quality improves at a minimal performance cost.

1. INTRODUCTION

Functional and parametric yield dominantly depends on patterns at 14/16 nm node and below. This dependency is due to subwavelength lithography and local layout effects, and it makes yield predictions more challenging [1]. At such advanced nodes, printed patterns can, significantly and non-systematically, differ from designed patterns due to neighboring effects. These lithographic errors [2] affect logic cells and they need to be characterized in silicon [3].

Silicon characterization can capture lithography-induced performance variation and hotspots in digital circuits [4]. However, characterizing a modern standard cell library is impractical due to following reasons. There are hundreds of cells and the possible vertical and horizontal abutment scenarios increase sharply with the library size.

In this paper, we propose a virtual characterization vehicle (VCV) methodology that can exhaustively evaluate all unique layout patterns as a function of a specified radius of influence (RoI) and layers of interest. By exhaustively searching for patterns, these VCVs compile pattern frequency for all possible cell combinations. VCV results can guide the design and selection of logic cells in a library based on their impact on DFM metrics. Moreover, these results can be used in silicon characterization to cover all possible layout patterns.

We demonstrate our results on a 14 nm cell library. Synthesis results show DFM quality improves at a minimal performance cost and, more importantly, VCV aided library design can reduce the number of patterns. Hence, silicon characterization with 100% pattern coverage becomes a reality.

2. VIRTUAL CHARACTERIZATION VEHICLE METHODOLOGY AND TOOL

Our proposed VCV methodology is a tool that takes a standard cell library as input and analyzes the patterns generated by abutment of cells. The tool analyzes the patterns of a library within a user specified window and for all layers of interest. For all of the experiments and results presented in this paper, a window size of 500nm x 500nm is considered. Window size (sometimes referred as clip size in the literature) is a function of the lithography process used and radius of influence. This radius is roughly 500 nm for 193 nm immersion lithography [5], which is the resolution enhancement technique used presently for the commercial 14/16nm nodes.

The front-end view (metal 2 and below) of a library can be used as the input to the tool. Since the 14nm FinFET technology considered relies on double patterning, the developed tool is color aware. It must be noted that poly layers and fin layers are already gridded for DFM compatibility, and therefore require no analysis.

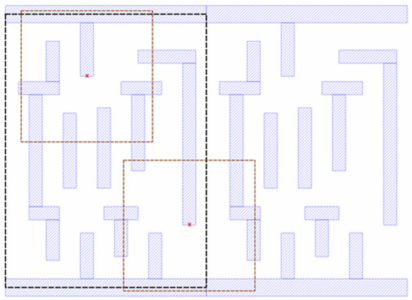

Figure 1. Windows of interest and their centering according to line-end patterns.

Figure 1 depicts two windows created by placing two 28 nm NAND cells side by side horizontally. Each window is centered on a red X marker. The blue rectangles are M1 shapes, and the dotted black line is the boundary of the analyzed cell. Location of X markers highly impacts the analysis. If markers were spaced by 1 nm (minimum drawn unit), window analysis becomes intractable, even for the smallest library. Alternatively, the VCV tool has two marker modes that are based on features instead of a grid. The first mode marks the center of a drawn shape, while the second mode marks the line-ends. Clearly the first approach is a fit for via layers, while both modes can be used for metal layers. Without loss of generality, the results presented in this paper always assume line-end markers for metal layers.

Two windows shown in Figure 1 are internal (top left) and external (bottom right). Internal windows are absolute for a cell whereas external windows depend on the abutment scenario. We also note that, for 28 nm, 500nm RoI contains up to 10 M1 routing tracks at minimum pitch. For 14 nm node this number goes up to 15 M1 tracks.

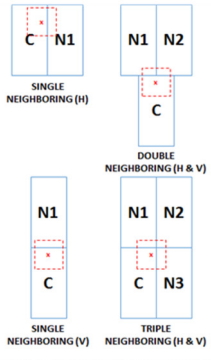

Figure 2. Neighboring possibilities and modes of operation.

The goal of the VCV tool is to evaluate all possible cell abutment scenarios, extract, and catalog all windows created from these scenarios. However, for a library of N cells, the number of possible scenarios is N^2 at minimum. This number climbs up if cell spacing is varied. A given pair of cells has approximately 30 horizontal abutment scenarios, when spaced at a multiple of the pitch. Vertical abutment, on the other hand, is more complicated and computationally expensive because one external window can include more than two neighbor cells. Therefore, we developed 3 distinct modes of operation: single, double, and triple. Figure 2 depicts all modes of operation. In the following chapters, we explicitly mention which mode is used for analysis. We should note that the triple mode can exhaustively capture all possible windows and exposes hotspots at the cost of high execution time.

The VCV tool catalogs windows depending on their occurrence frequency. It is important to capture frequent windows and more important to capture the ones that appear only once. Windows that occur once are named a Single Occurrence Windows (SOWs) whereas windows that occur more than once are named a Multiple Occurrence Windows (MOWs).

3. VCV ANALYSIS OF A 14NM LOGIC CELL LIBRARY

A 14 nm FinFET, single 9-track standard cell library was used in this section. The library is composed of more than 800 cells, majorly combinational cells. Metal pins are drawn in either M1 or M2. Less than half of the cells have M2 routing, typically the complex ones. For analysis, all possible horizontal abutment scenarios were considered, whereas only single neighboring was considered for vertical interaction.

Figure 3 depicts our first analysis of the library, in which metal layer 1 (M1) is considered. The image shows 3 lines: a red line for the total number of windows, a green line for SOWs, and a blue line for MOWs. The total number of windows is the sum of SOWs and MOWs. This analysis is

cumulative and the cells are analyzed in alphabetical order. The vertical axis is the number of windows in millions, whereas the horizontal axis shows library cells. This library contains 40 million M1 windows and one-fourth of them are SOWs.

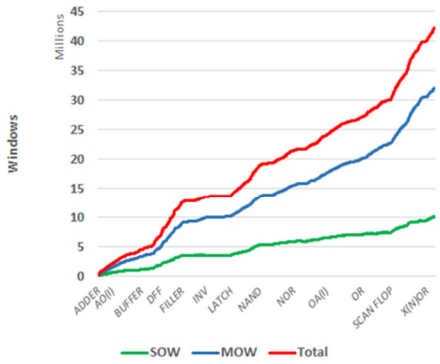

Figure 3. Accumulated analysis of windows for the M1 layer.

Specific regions of Figure 3 are of interest. First, we note how flip-flops (DFF and scan) interact with the other cells in the library and create a high number of windows. This happens because these wide cells imply more vertical abutment scenarios. Like DFF, even a single cell family can rapidly change the slope of the curve that affects DFM quality. On the other hand, the curve remains flat for filler cells that contain simple, common and regular layout patterns. We observed the same profile with inverter cells as well.

The silicon area needed to characterize the whole library is determined by the total number of windows. Therefore, the number of total windows is a clear *metric of interest*. However, some of these windows appear multiple times and merit a proper characterization, while SOWs appear once and yet still require the same characterization effort. Therefore, SOW ratio is a *metric of interest* for DFM quality. Figure 3 shows a concerning trend: the number of total windows keeps growing as more cells are added to the already known set of windows. So does the number of SOWs.

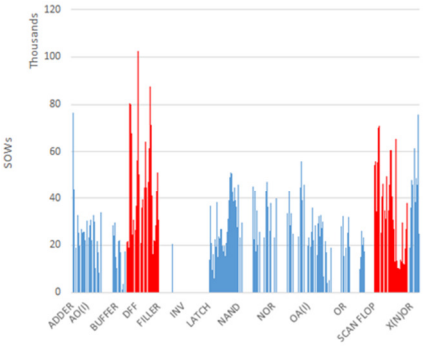

Figure 4. M1 analysis of SOWs created by each cell.

Every cell contributes differently to the total number of windows. Figure 4 represents SOWs injected by each cell type. As a single DFF can create up to 100k SOWs, all DFFs account for 32% of all SOWs. Therefore, DFFs, frequent elements of digital blocks, need to be carefully designed to minimize SOWs; hence, total number of windows.

4.LIBRARY COMPOSITION

We synthesized circuits from IWLS05 [6] to evaluate the pattern count, which correlates with DFM quality, based on library composition. These circuits are benchmarks obtained from opencores.org.

Our baseline for comparisons is the same commercial library and we refer to it as LIB_BL. LIB1, the smallest subset of LIB_BL, contains mandatory and frequently used cells. LIB1 has a total of 65 cells; 7 physical cells, 11 buffers of different strengths, 9 sequential cells (only X1), and a variation of combinational cells of X1 strength. LIB2 differs from LIB1 by 6 sequential cells with higher driving strengths. Moreover, LIB3 is a superset of LIB2 with 9 additional combinational cells with higher driving strengths.

We synthesized the selected benchmarks for each library; LIB_BL, LIB1, LIB2, and LIB3. The same optimizations (clock gating, high effort mapping, etc.) are applied across all circuits and ideal clocks were used for all experiments, i.e., no jitter or skew was considered.

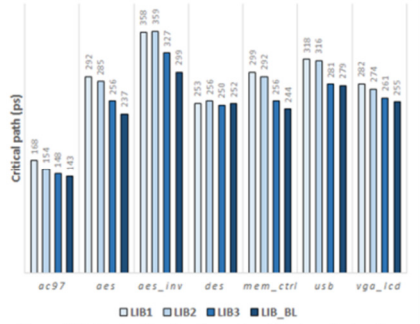

Figure 5. Critical path values for various benchmark circuits.

Figure 5 shows the critical path for benchmark circuits. Generally speaking, *carefully selected* cells help synthesis tools to achieve a better timing. On average, LIB1 circuits have critical paths that are 15.4% slower than their LIB_BL counterparts. With the additional cells in LIB2, this difference drops to 12.8%. Finally, with LIB3 expansion, this difference drops to only 4.0%. The slowest critical path with LIB3 is in *aes_inv* circuit, which is 9.3% slower than LIB_BL. However, the same circuit, when implemented with LIB1 or LIB2 is approximately 20% slower, showing LIB3 was meaningfully expanded.

We should note that Figure 5 represents the critical path results for nominal corners. However, as far as variability concerned, libraries like LIB_BL have to account for diverse neighboring scenarios and associated uncertainties through pessimistic assumptions. Libraries with fewer patterns; hence a tighter statistical distribution, allow less pessimistic worst case scenarios.

Power and area measurements for given benchmarks do not show clear increasing or decreasing trends; hence, they were not represented.

Library	Total M1 windows (millions)	Estimated silicon area (mm^2)
LIB_BL	>10000 (*)	>40000 (*)
LIB1	19.1	77.0
LIB2	21.2	85.4
LIB3	32.4	130.6

Table 1. Estimated silicon area required to precharacterize all M1 windows obtained by triple neighboring.

5.CONCLUSION

Our VCV methodology exhaustively evaluates all abutment scenarios for a standard cell library and shows the DFM quality of a library (SOWs and MOWs) and helps estimating the silicon area required to test these scenarios. Our results show that smaller libraries can improve DFM quality at a modest performance cost. Additionally, VCV methodology exposed that DFF can introduce many new windows. This is an exact goal of this paper because only an exhaustive VCV can expose these cells in a timely fashion so that they can be redesigned and/or completely eliminated from a library. Furthermore, Table 1 demonstrates that covering all possible abutment scenarios in silicon is practically impossible for a library with diverse libraries such as LIB_BL. On the other hand, the same table suggests that smaller libraries (LIB 1, 2, and 3) can be analyzed for DFM quality at a reasonable expense. VCV methodology is an invaluable tool because future technology nodes such as 10nm and 7nm are likely to still use 193nm immersion lithography with deeply scaled dimensions. Therefore, the window size to minimum pitch ratio is expected to grow, increasing the relevance of having a VCV methodology that allows design of libraries that can feasibly be characterized in silicon.

6.ACKNOWLEDGEMENTS

This work was supported in part by DARPA contract HR0011-16-C-0038, Circuit Realization At Faster Timescales (CRAFT).

7.REFERENCES

[1] Gupta, P. and Kahng, A. B. Manufacturing-aware physical design, ICCAD'03. pp. 681-687.
[2] Xu, X., Cline, B., Yeric, G., Yu, B., Pan, D. Z. Systematic framework for evaluating standard cell middle-of-line robustness for multiple patterning lithography. J. Micro/Nanolithography, MEMS, and MOEMS. (Feb 2016). DOI=10.1117/1.JMM.15.2.021202.
[3] Cao, K., Dobre, S., and Hu, J. Standard cell characterization considering lithography induced variations. DAC.2006.
[4] Ghan, J., et al. Clustering and pattern matching for an automatic hotspot classification and detection system, Proceedings of SPIE2009
[5] Orshansky, M., Nasif, S., Boning, D., "Design for manufacturability and statistical design: a constructive approach," p. 130, 2008.
[6] IWLS 2005 Benchmarks. http://iwls.org/iwls2005/benchmarks.html