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3.125GS/s, 4.9 ENOB, 109 fJ/Conversion Time-Domain ADC for Backplane Interconnect

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Abstract. This paper presents a flash Time Domain ADC with T/H amplifier, Voltage Controlled Delay Line and Time to Digital Converter. The design is operating at 3.125GS/s with 4.9 ENOB and a Walden figure of merit of 109fJ/Conversion. Automatic calibration means are provided as well. For measurements purposes, an integrated memory is provided. It consumes 16.2mW from a 1V supply. It was realized in the 45nm PDSOI from Global Foundries.

Keywords: Sampler, Track and Hold, Time-Domain ADC, Backplane interconnect, Gigabit Radio, mm-Waves

1 Introduction

The progression of Time Domain ADCs, marked by improvements in sampling rates, energy efficiency, and integration capabilities, highlights the progress of the research community, paving the way for their widespread adoption in future digital systems. Further more, new research areas in mm-wave wireless communications on 5G at 28GHz, cognitive radios, 60GHz (802.15.3.c, ECMA-387, WiHD standards), and mobile/cable television require a broadband ADC converter with bandwidths in excess of 850MHz and moderate accuracy (7-10bits) for digitizing the IF signal and/or direct sampling at RF. Other applications are backplane interconnect with digital equalization that require a 4-5 bit A/D converters, emerging technologies, particularly in high-speed communications and IoT devices and LIDAR. The new applications require high linearity at high sample rates ($fs > 2Gs/s$) with large bandwidth and low power consumption [1–4]. Time Domain ADC systems serve as alternatives to Voltage Domain ADCs, primarily due to the low voltage requirements of contemporary technologies, often below 1V. This lower voltage threshold exacerbates the issue of offset voltages in ADC design, where even a 9-bit converter's least significant bit (LSB) nears 1.95mV, close to the offset and noise levels. Time Domain ADCs, utilizing Time to Digital Converters (TDC), offer a solution by quantizing time intervals instead of voltages, providing superior time resolution. This approach is particularly advantageous when the input signal is capped at 1V, aligning with the

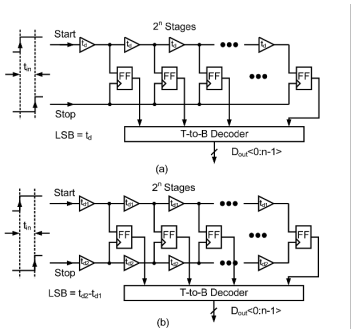

Fig. 1. (a) Delay line ADC, (b) Vernier TDC

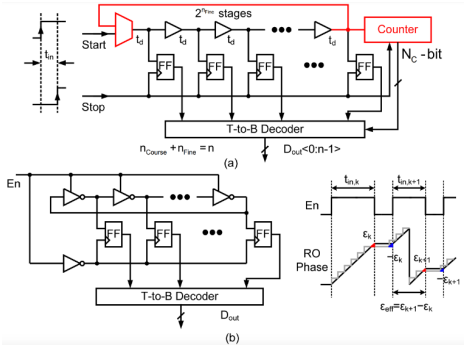

Fig. 2. (*a*) Ring based TDC (b) gated RO TDC with noise shaping

reduced supply voltages in modern circuits. The paper highlights a novel Time Domain ADC that incorporates a Voltage Controlled Delay Line (VCDL) for enhanced linearity and introduces an innovative TDC structure, noted for its area efficiency and rapid processing capabilities.

1.1 Overview of Time Domain ADCs

In the realm of Time Domain ADCs, Flash TDCs, recognized for their delay-line architecture, face scalability issues due to the increased need for inverters and comparators as resolution grows. To address these limitations, two innovative approaches are introduced. Notably, the Vernier TDC method, which leverages a pair of delay lines with varying stage delays, significantly improves the precision of timing difference measurements. This advancement in accuracy, facilitated by the careful calibration between the two lines (see Fig. 2), marks a pivotal step in overcoming the inherent constraints of gate delay resolutions.

By using the dual delay lines with variable stage delays, the Vernier and Pulse Shrinking (PS) TDC methods facilitate the attainment of smaller LSB sizes, albeit at a cost of greater power and spatial requirements Fig. 1. The PS TDC method [5, 6], in particular, achieves this by exploiting the delay variations between buffer transitions. However, these techniques encounter challenges, including poor matching that renders conventional averaging methods ineffective, resulting in significant DNL/INL issues [7, 8], and reduced conversion speeds, which limit their application in high-speed environments. Furthermore, their increased power demands, especially in less demanding operations, present obstacles to efficiency and performance in sophisticated circuit designs.

Streamlining TDC designs using ring oscillators simplifies signal folding within the time domain. This method, by integrating RO in precise TDC configurations alongside counting mechanisms or separate coarse TDCs, creates a foldable TDC model that matches Flash TDCs in speed but with fewer delay stages and DFFs Fig. 1. RO edge transitions enhance phase interpolation, improving LSB precision and matching. Gated-RO (GRO) TDCs introduce noise shaping and energy

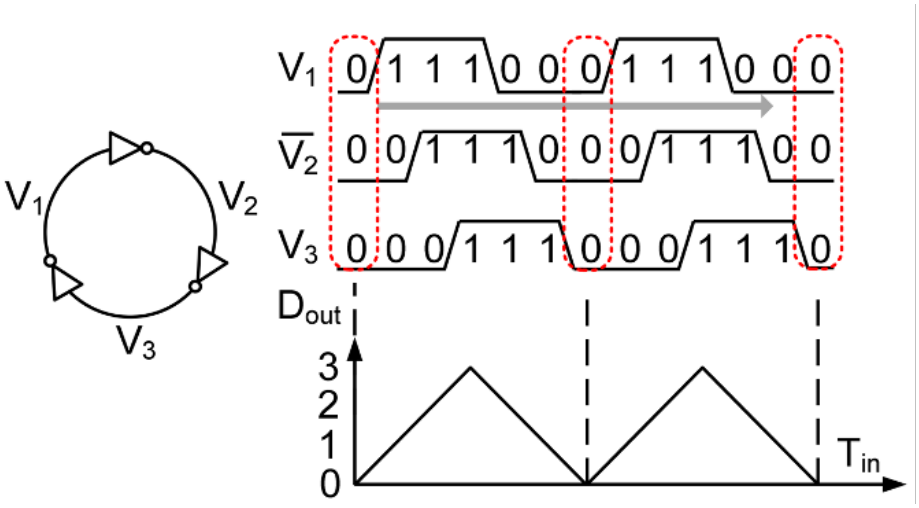

Fig. 3. Differential T/H amplifier with charge compensation

efficiency, achieving higher SNR through oversampling [9]. However, GRO TDCs face leakage issues due to reliance on internal node capacitance, a problem addressed by Switched RO (SRO) TDCs [10, 7].

Similar to Flash ADCs, Flash TDCs and RO-based TDCs exhibit a direct exponential relationship between their resolution and conversion speed, presenting a challenge for achieving high resolution quickly. Addressing this, advanced two-step or pipelined TDC designs with time amplification and multiple stages have been developed, capable of reaching resolutions over 9 bits at speeds in the hundreds of megahertz. The incorporation of a time amplifier (TA) is crucial in these designs, although the complexity of implementing a Multiplying Digital-to-Time Converter (MDTC) introduces difficulties, such as the need for extensive dummy delay stages or conversion back to the voltage domain, to store time residue effectively.

The SAR TDC eliminates the need for time amplification, allowing for finer LSB precision [11, 12]. However, managing residue signals in the time domain poses a challenge. A method involves adding dummy delay stages next to the main path, using multiplexers to select edges for residue signals, leading to significant dynamic power consumption [11]. An alternative involves incorporating SAR logic into a Gated Ring Oscillator (GRO) with correlated double sampling, offering a different approach to address these challenges.

Utilizing a three-stage Ring Oscillator (RO) as exemplified, this approach captures periodic waveforms across nodes V1, V2, and V3, forming a thermometer-like digital sequence that iterates through six states each RO period. This technique, benefiting from noise shaping through oversampling, boasts the dual advantages of compactness and swift operation [13]. Unlike traditional methods that rely on power-intensive dummy stages for storing time residue, this strat-

egy accumulates the residue signal incrementally, ensuring each transition in the thermometer sequence accurately reflects the quantizer's LSB magnitude, thereby enhancing time-domain folding's efficiency.

Hence, the RO achieves a streamlined approach to signal folding and quantization within the time domain. With an N-stage RO, the system can cycle through 2N states. This method offers two key benefits over voltage domain folding. Firstly, while voltage domain operations often suffer from non-linearity, necessitating parallel folding techniques [61] that introduce significant complexity, time-domain folding via RO maintains inherent linearity due to the cyclical phase changes without edge effects. Secondly, time-domain folding can theoretically achieve unlimited folding factors given sufficient conversion time, unlike voltage domain methods constrained by the number of available folding amplifiers.

In conclusion, the exploration of Time Domain ADCs, particularly Flash TDCs, RO-based TDCs, and Vernier and Pulse Shrinking TDCs, highlights the key tradeoff metrics such as resolution, speed, and power efficiency essential in many ADC architectures. These advancements set the stage for delving into Voltage-Controlled Oscillator (VCO) based Delay Line TDCs, promising further optimizations in the domain of high-speed and high-resolution analog-to-digital conversion, which will be the key theme of our next discussion.

1.2 Voltage Controlled Delay Line Based T/H

The Time Domain A/D converter system is shown in Fig. 4. This type of ADC relies on a Time to Digital Converter (TDC) to generate a digital output. Instead of quantizing a voltage this ADC quantizes a time interval. The differential T/H amplifier is shown in Fig. 5.

Transistors M2, M3, M2' and M3' are half width transistors and used to compensate for CK injection in the switch M1 and M1'. The transistors M4 and M4' are compensating input/output feedthrough. The T/H amplifier cannot directly drive a Time to Digital Converter (TDC). Before the Time to Digital

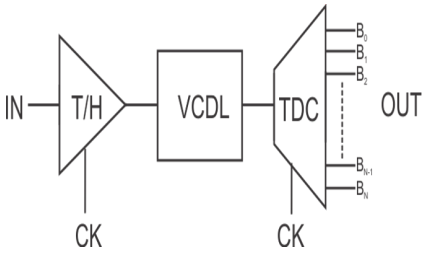

Fig. 4. Voltage to time converter preceding TDC in a TAD

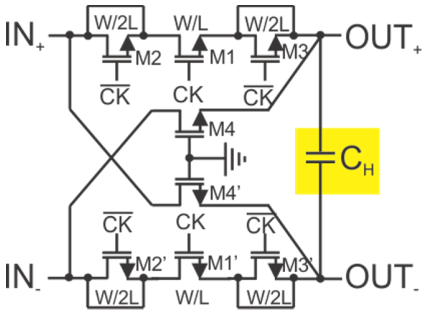

Fig. 5. Differential T/H amplifier with charge compensation

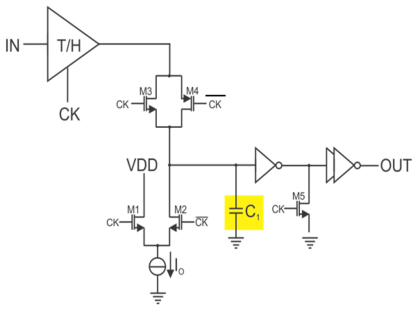

Fig. 6. Differential T/H amplifier with charge compensation

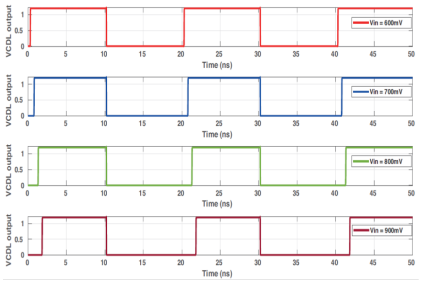

Fig. 7. The output of the VCDL for different input voltages

Converter (TDC) we need a voltage to time converter that can be realized as a voltage-controlled delay line as in Fig. 6.

The capacitor C1 is charged from the input voltage and discharged from a constant current source. When clock CK is high, the switch M3 is on and the input voltage from the T/H is charged on the capacitor C1. When CK is high, the switch M5 is ON and the output of the inverter is forced to 0, M1 is ON and the current Io is directed to the supply VDD. This leads to undetermined signal components in the voltage over the hold capacitor.

When CK is low, the switches M3, M4 are off and the switch M2 is ON and the current Io discharges the capacitor C1. When the voltage on the capacitor reaches VDD/2, the inverter will switch from 0 to 1. As the switch M5 is OFF, the output of the inverter will generate a pulse with the length proportional to the input voltage Vin from the T/H output. This pulse is applied to a chain of buffers that goes to the TDC input. The simulated output of the Voltage Controlled Delay Line. (VCDL) is presented in Fig. 7. Four different input voltages of 600mV, 700mV, 800mV and 900mV respectively are applied to the input of the VCDL. The pulse width depends linearly on the input voltage. We get a pulse width modulator. The linearity of the VCDL is very important for the linearity of the TADC. For 8-9 bit accuracy, the linearity of the VCDL should be better than the 8-9 bit linearity of the TADC system. In the remainder of the paper we are introducing the Time Domain ADC Architecture and measured results.

2 3.125GS/S 4.9 ENOB TIME-DOMAIN ADC

TDC is based on voltage-controlled delay lines (VCDL) and Vernier TDC with sign and magnitude.The block diagram is shown in Fig. 8 The input is applied to a linear T/H amplifier (see Fig. 5). The two differential signals from S/H, VP and VN, are applied to two voltage-controlled delay lines (VCDL) (see Fig. 8). The main idea behind conversion is inserting a known clock edge to the delay line (in this case CKADC) and generating OP and ON transitions with delays proportional to VP and VN voltages respectively. Comparing the arrival time

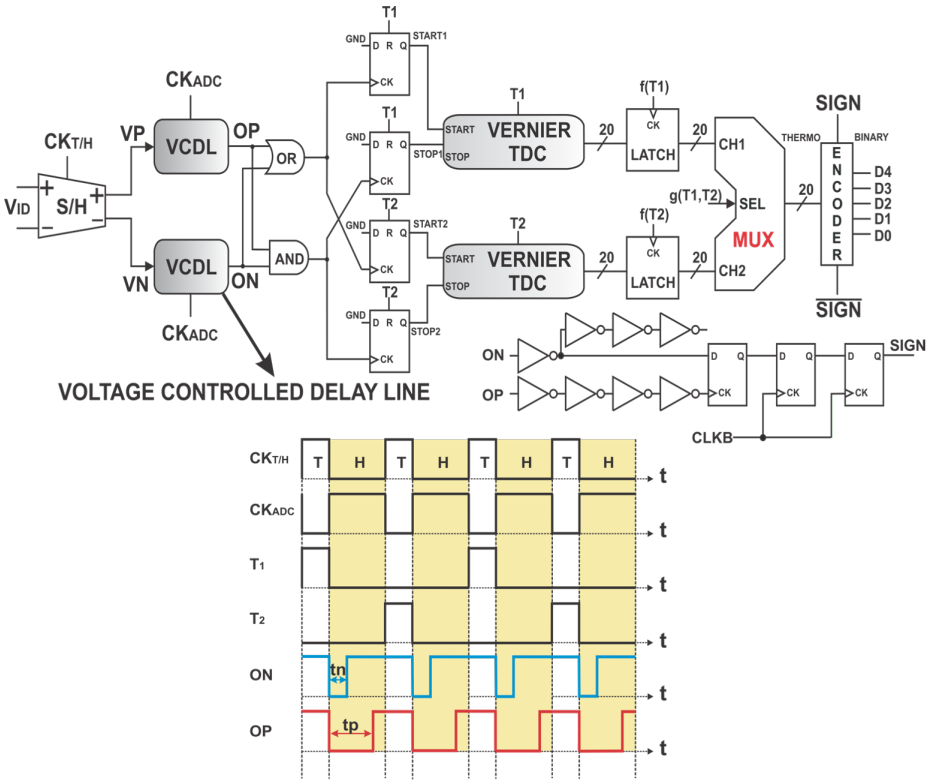

Fig. 8. TDC architecture

of OP and ON signals we generate a sign bit. To resolve the other 4 bits, the Vernier TDC measures the time difference between OP and ON transitions. The START signal of the TDC is the one that is generated faster at the output of VCDL and the STOP signal is the slower one which corresponds to the larger input. START signal can be the OR function of OP and ON and STOP signal can be the AND function of OP and ON. In order to have the delay range as wide as possible, we delay the clock in the VCDLs through some buffers to pre-charge the stages sequentially and give more time to the slower signal before it gets destroyed in pre-charging process. In the worst case, the STOP signal can be very short and cannot be properly sampled by a flip-flop at the output of the TDC. The purpose of the two flip-flops at the output of OR and AND gates is to sample the START/STOP edges. In order to relax timing issues we use two TDCs that toggle between the sampling flip-flops and keep their outputs for one more cycle. This comes at the expense of two clock period latency to have the output ready. The outputs of the two TDCs are latched and MUX-ed to the encoder. The SIGN bit decides if a particular output has to be inverted or not in order to get a sign and magnitude binary output. The TDC is shown in Fig. 9.

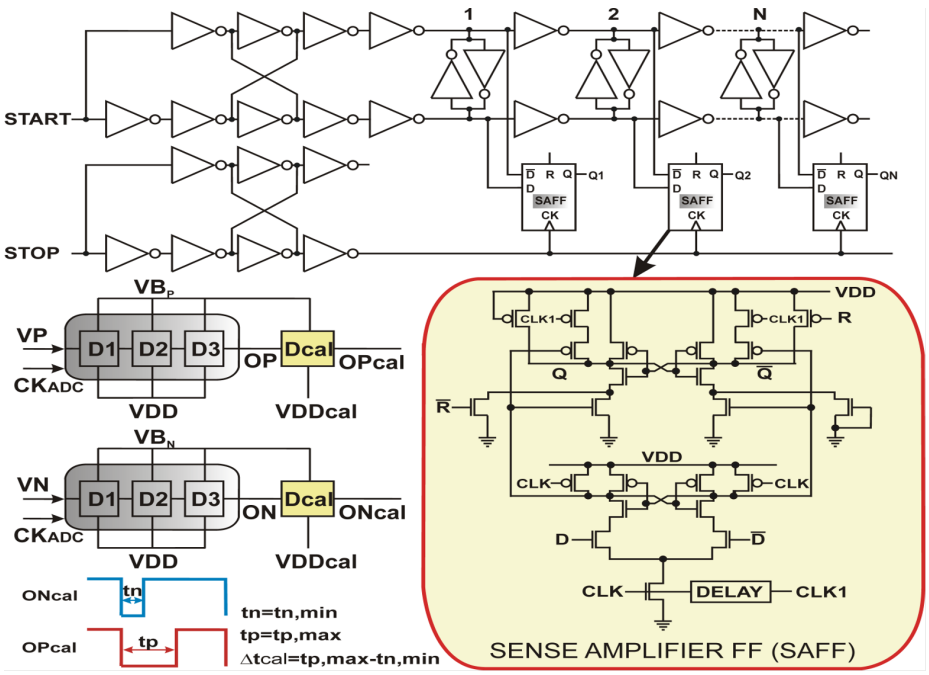

Fig. 9. Vernier TDC, sense amplifier flip-flop and calibration principle

The faster signal, START, is inverted through an edge aligner and the two polarities go through a chain of inverters.

The inverter delay defines the resolution of TDC. The START signal and its opposite polarity travel through the inverters and the slower signal STOP samples the delayed signals. To keep the delay between START and STOP the same the STOP signal goes through the same edge aligner.

Back-to-back inverters are used for de-skewing the outputs of inverters in the delay line. They add extra delay to inverter delays but they control the falling and rising edge skew in case of process matching. The delay line inverters are tuned through the supply voltage. The sense-amplifier flip-flops Fig. 9 are based on SR flip-flops clocked with the delayed version of the main clock to reduce the meta-stability window. For calibration, the VCDLs have an extra delay cell Dcal with their own supply. The input of the S/H has maximum differential imbalance and the outputs of the extra delay cells experience a short ONcal pulse (tn=tn,min) and a long OPcal pulse (tp=tp,max). The phase of a known clock signal (fCLK=2xfs) is adjusted to align its rising edge on the ONcal edge. We change then VBP of the VCDL to align the OPcal transition on the second clock rising edge. With differential delay calibrated we change the TDC supply to get code “15” at the encoder output. The TDC described above, along with a serial interface to support control functions, were implemented in a GF 45nm SOI CMOS process. Figs. 10 and 11 shows the measured DNL and INL before and

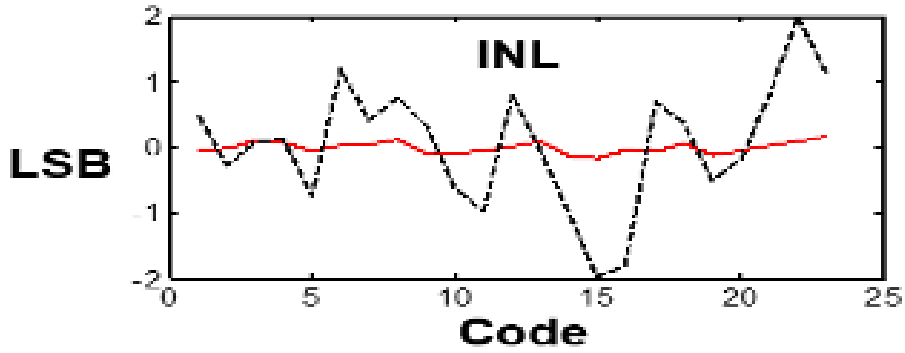

Fig. 10. Measured INL of the TADC

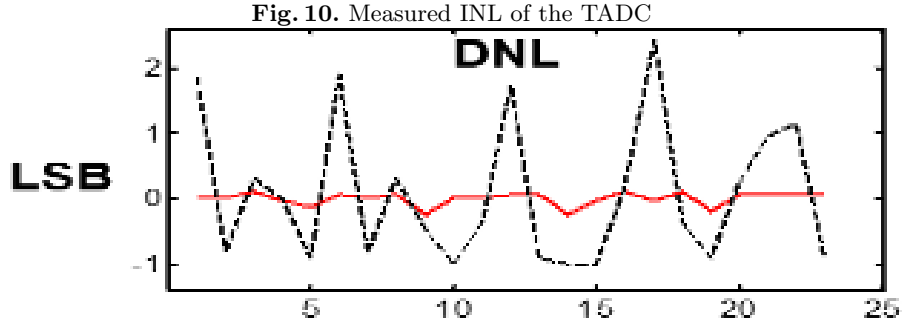

Fig. 11. Measured DNL of the TADC before (black) and after calibration(red)

after calibration and Fig. 12 show the ENOB of about 4.5 across the frequency of interest.

The Walden FOM [14] for the TADC is 109fJ/conversion Fig. 13. For linearity measurements, we apply two input tones at 320MHz and 400MHz. For an input power of -16.98dBm, the measured IIP3 is IIP3=-16.98+28/2=-2.9dBm. The output spectrum is shown in Fig. 15 and the measured eye diagram of an equalized lossy backplane interconnect (with FFE and DFE 5) is shown in Fig. 14. To put things in perspective, Table 1 presents a benchmark with other comparable A/D converters from literature.

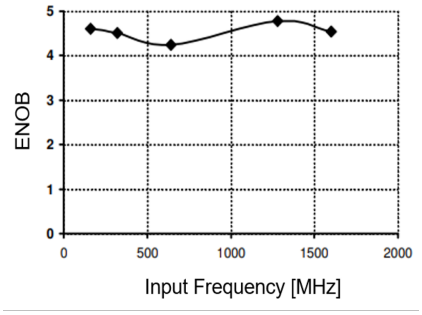

Fig. 12. ENOB variation with frequency

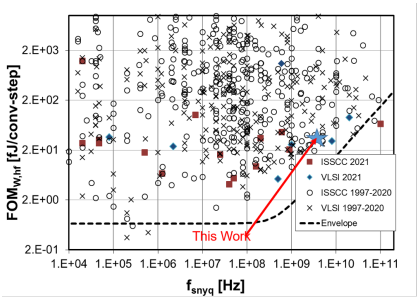

Fig. 13. Benchmarking based on Walden FOM from [15]

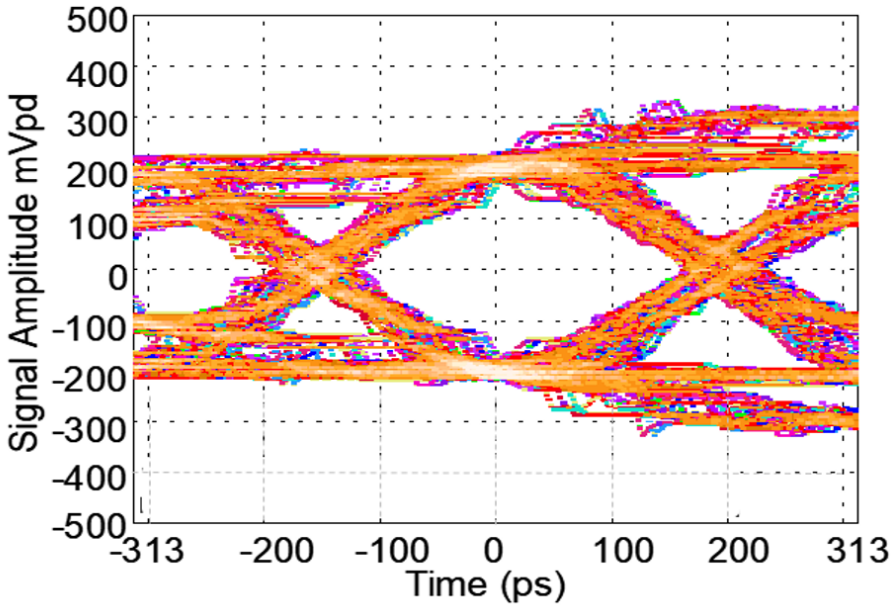

Fig. 14. Measured eye diagram for a 3.2Gs/s data

The A/D converter from [2] has a FOM of 59.4 fJ/Conversion. Our design has a better DNL and INL after calibration. The A/D converter from [2] has a FOM of 40 fJ/Conversion but the DNL and INL are 0.8 LSB. The A/D from [9] has a FOM of 109 fJ/Conversion but no DNL is reported. The reference [6] reports a FOM of 910fJ/ Conversion. The A/D from [9] reports a FOM of 143fJ/Conversion.

Table 1. Performance Summary and Comparison with the State of the Art

Parameter	This work	[15]	[2]	[6]	[5]	[9]
Year	2023	VLSI 2013	JSSC 2010	VLSI 2012	JSSC 2011	VLSI 2015
Process Technology	45nm PD-SOI	32nm SOI	40nm CMOS	40nm CMOS	65nm CMOS	65nm CMOS
Architecture	Time Domain	Flash	Pipelined	Flash	Flash/Interleaved	Interleaved
Sample Frequency	3.2 GS/s	5 GS/s	2.2 GS/s	3 GS/s	16 GS/s	25 GS/s
ENOB	4.9	6	6	6	4.9	4.62
DNL	0.1 LSB	0.52 LSB	0.8 LSB	N/A	< 0.5 LSB	0.35 LSB
INL	0.1 LSB	0.37 LSB	0.8 LSB	0.35 LSB	< 0.5 LSB	0.39 LSB
Power Consumption	16.2 mW	8.5 mW	2.6 mW	11 mW	435 mW	88 mW
Chip Area	0.049 mm^2	0.03 mm^2	0.03 mm^2	0.021 mm^2	1.42 mm^2	0.24 mm^2
FOM	109 fJ/Conversion	59.4 fJ/Conversion	40 fJ/Conversion	109 fJ/Conversion	91 fJ/Conversion	143 fJ/Conversion

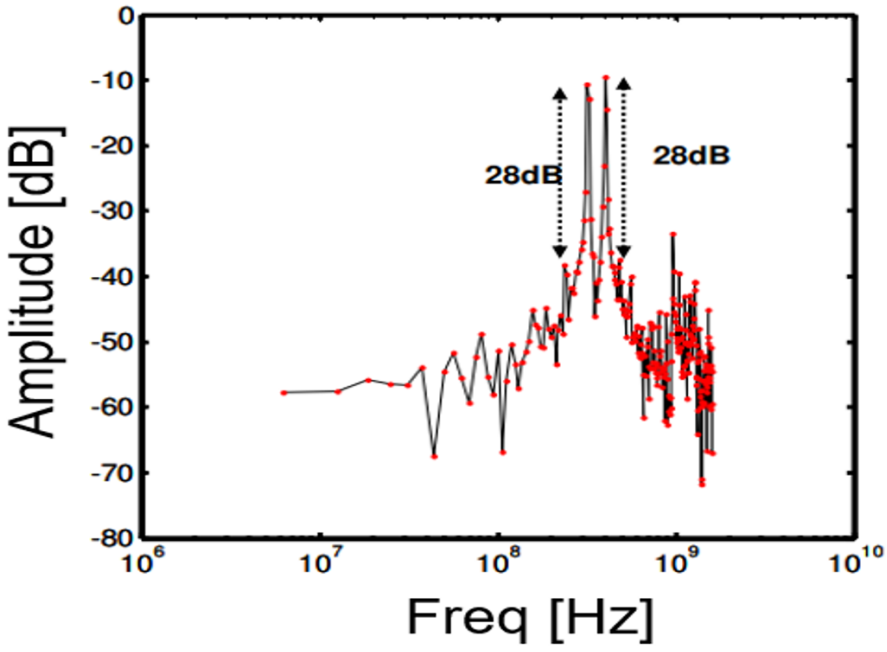

Fig. 15. Signal Amplitude

Our design compares well with other designs from literature and has a better FOM than other designs for the same sample rate and ENOB. Signal amplitude of the data at 3.2G is shown in Fig. 15. and the chip photomicrograph is presented in Fig. 16.

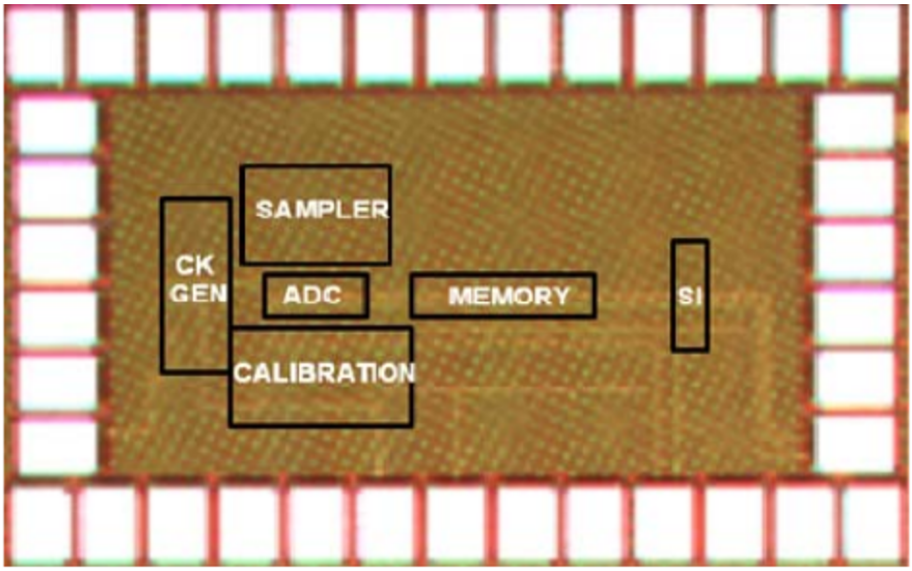

Fig. 16. Chip Micrograph

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