



A Silicon-Based Fanout Technology with High Aspect Ratio TSV for RF Heterogenous Integration Applications

Jiao Zonglei, Li Jie, Wang Zhengyan and Zhang Hongze

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A silicon-based fanout technology with high aspect ratio TSV for RF heterogenous integration applications

Zonglei Jiao*

Nanjing Electronic Devices Institute
NanJing, China
scientistjzl@163.com

Jie Li

Nanjing Electronic Devices Institute
NanJing, China
990323601@qq.com

ZhengyanWang

Nanjing Electronic Devices Institute
NanJing, China
zywang0405@163.com

Hongze Zhang

Nanjing Electronic Devices Institute
NanJing, China
zhanghongze007@pku.edu.cn

Abstract—Advanced packaging technology has demonstrated its unique technical advantages in miniaturization and high-density integrated application of RF Microsystems. Among many advanced packaging technologies, fan-out packaging technology has been widely used in recent years because of its advantages of high integration, high fabrication flexibility, simple process and low process cost. However, the traditional fan-out wafer-level package (FOWLP) and fan-out board-level package (FOPLP) are mainly aimed at CMOS chip packaging applications, and they face many technical problems in compound RF chip packaging applications, such as RF grounding, heat dissipation of high-power RF chips, air bridge protection of RF chips and signal transmission in vertical. In view of the above problems, this paper proposes a fanout technology based on silicon-based TSV interposer. By making silicon-based interposer with two different depths of TSV, deep TSV is used for vertical interconnection of signals, and shallow TSV is used for grounding of RF chips. After the interposer is prepared, a cavity is dry etched on the back of shallow TSV for chip embedding. The chip is bonded in the cavity with conductive adhesive with high thermal conductivity. After the bonding process, the vacuum gluing technology is used to spin-coat polyimide as a passivation isolation layer between the chip and the RDL layer. In this paper, a silicon-based Fanout integration of GaAs chip has been successfully fabricated, and the RF performance has almost no attenuation compared with the die mounting test. Results On the surface, the silicon-based fanout technology proposed in this paper can realize the lossless packaging of compound chips with air bridge structure, and has good grounding and heat dissipation performance, which has obvious technical advantages compared with the traditional Fanout technology.

Keywords— Fanout, RF Microsystem, TSV Interposer

I. INTRODUCTION

With the development of unmanned aerial vehicle (UAV), precision guided weapons and other technologies, the demand for miniaturization of RF modules is becoming more and more urgent, and RF micro-systems are developing in the direction of miniaturization, multifunction and high reliability. The traditional metal shell packaging can't meet the miniaturization demand of electronic equipment in the future. At present, the fan-out board-level packaging has some technological problems such as warping and mold displacement[1][2], and there is no effective solution to the problems of RF grounding and high-power heat dissipation, which limits its application in RF packaging.

In view of the future development requirements of RF Microsystems technology, proposes a silicon-based Fanout technology based on TSV interposer, which realizes the vertical interconnection of signals and the nearby grounding of chips through two different depths of TSV. The heat dissipation problem of high power chip is solved by the high thermal conductivity of silicon and the unique chip bonding method. The problem of extrusion deformation of the surface structure of compound chip is solved by vacuum coating technology of passivation layer polymer material. By using the process based on silicon wafer, the problems of warping, precise alignment of chip pads and mass production are solved. Through the above key technologies, the difficult problem of RF chip packaging is well solved. The process technology system mainly includes key processes such as etching of TSV with different depths, electroplating of TSV with different depths, precise alignment and mounting of chips, vacuum coating of polymer medium, etc. This study solved the above technical problems through technical research, opened up the whole process flow and verified the feasibility of the process by packaging a compound chip with silicon-based Fanout technology.

II. PROCESS FLOW

The process flow of silicon-based fanout for compound chip packaging studied in this paper is shown in Figure 1:

1. Blind hole etching with two different depths
2. Copper electroplating filling of blind holes
3. Preparation of the back RDL layer and wafer thinning.
4. Etching the embedded cavity of the chip
5. Preparation of ground plane RDL
6. Chip embedding and mounting
7. Coating of passivation layer
8. Passivation layer graphics
9. Preparation of front RDL layer

The sample is completed through the above process flow. Among them, two kinds of hole etching with different depths, copper electroplating filling and coating of passivation layer are the key processes and technical difficulties of this process, and the following focuses on these key processes.

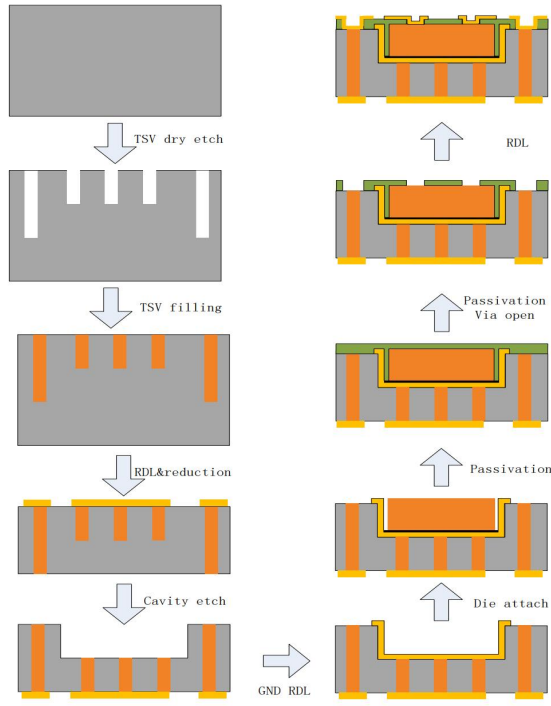


Fig. 1. process flow of silicon-based Fanout

A. Two deep hole etching technologies

Usually, two kinds of structures with different depths need to be etched in stages [3]. First, an etching mask is made to etch one structure; Then another structure is made by removing the first etching mask and then making the second etching mask. When using this scheme to prepare the structure in this study, it is difficult to choose a mask material to realize the complete coverage protection of the blind hole because of the large depth-width ratio of TSV (6:1~10:1), which causes the second etching to have a certain impact on the results of the first etching.

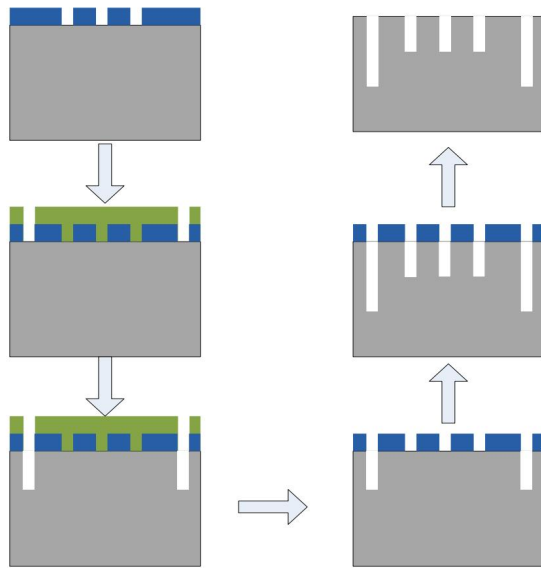


Fig. 2. process flow of deep and shallow hole structure

In this study, a method of combining hard mask with photoresist mask is used. As shown in Figure 2, firstly, an

oxide layer is grown and the shallow hole structure is patterned as a shallow hole dry etching mask, then a deep hole etching mask is made by using photoresist, and then the oxide layer etching and the preliminary etching of the deep hole are carried out. The etching depth needs to be determined according to the etching rate and the target value of the shallow hole etching. In this study, the etching depth of the deep hole is 200um, and the etching depth of the shallow hole is 100um. According to the etching rate, the deep hole is etched to $140\mu\text{m} \pm 5\mu\text{m}$, and then the photoresist mask is removed. The etching time is calculated, and the shallow hole is etched to a depth of 100um, and the depth of the deep hole is tested to be $200\mu\text{m} \pm 10\mu\text{m}$. Then the silicon oxide is removed to obtain the designed deep and shallow hole structure.

B. electroplate filling of deep and shallow hole structure

Conventional TSV electroplating process [4] is difficult to completely fill deep and shallow holes by changing the current. It is difficult to achieve relative stability in different holes due to the influence of hole morphology, local electric field, liquid flow rate, additive concentration, etc. According to the filling demand of deep and shallow holes in this study, it is considered that the main reason for not filling is the poor consistency of drug density distribution in holes. By improving the flow field and the exchange in the hole, and at the same time using the variable- current electroplating method, after the shallow hole is filled to the surface, the electroplating rate drops rapidly due to the effect of the surface inhibitor [5], while the deep hole electroplating rate is basically unaffected. By increasing the electroplating time, the two holes are finally completely electroplated, and the electroplating effect is shown in Figure 3.

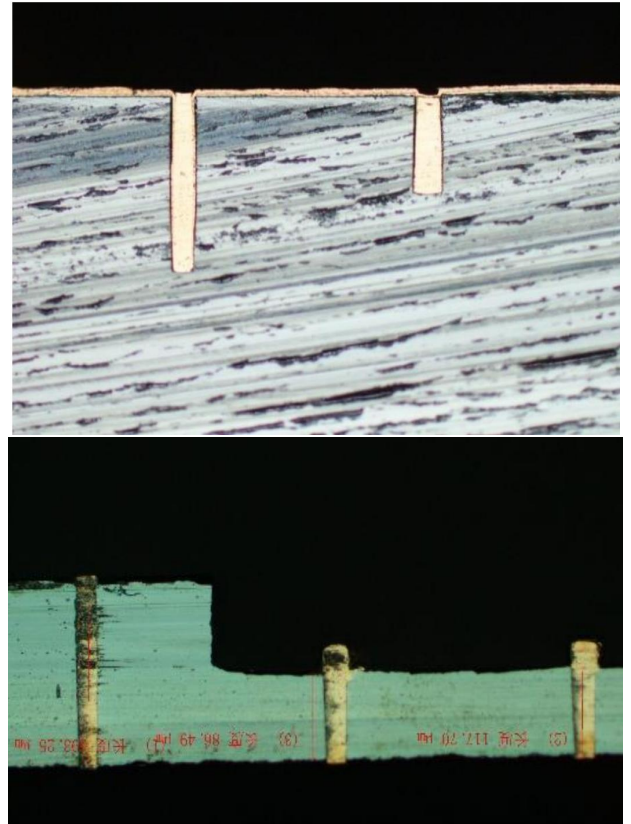


Fig. 3. Deep and shallow hole electroplating filling sample

C. coating the passivation layer medium PI

In order to completely fill the gap between the chip and the cavity, and at the same time protect the suspended structure on the chip surface from extrusion deformation, in this study, vacuum gluing technology is used to coat the surface of the wafer with polyimide[6][7][8], and vacuum gluing technology can completely fill and flatten the tiny gap. The process is shown in Figure 4:

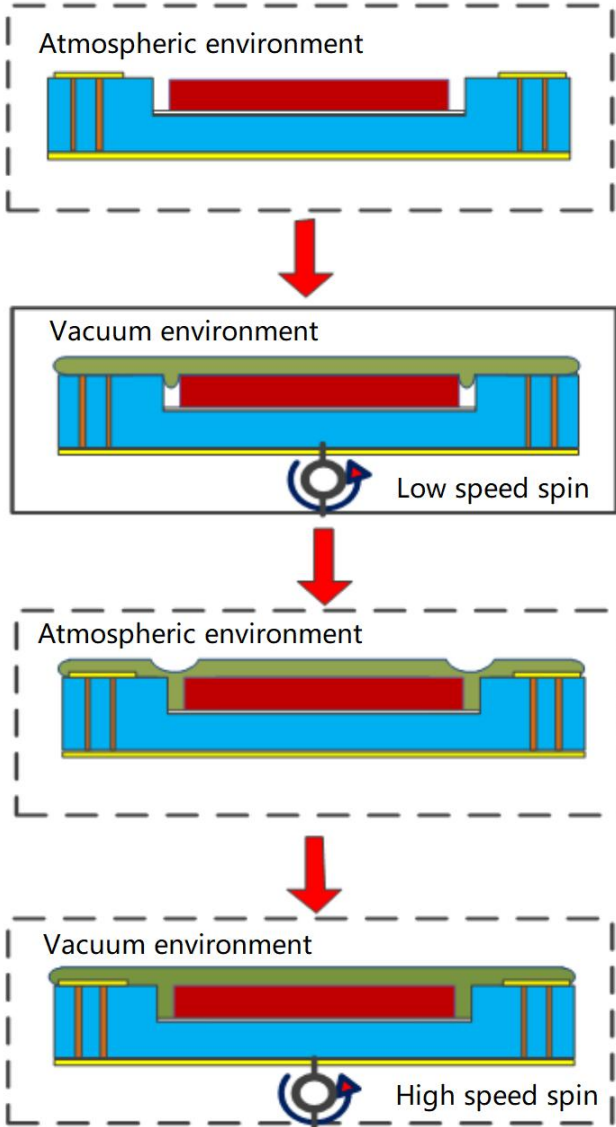


Fig. 4. process flow of vacuum gluing

Firstly, low-speed glue coating is carried out on a wafer containing tiny gaps in a vacuum environment; After gluing is completed, the vacuum is broken, and the glue is pressed into the gap by atmospheric pressure, so that the surface of the glue at the gap will be uneven; Finally, in the normal pressure environment, high-speed spin coating is carried out to flatten the adhesive surface. After gluing, the photoresist is cured at a certain temperature. After the curing is completed, the planar process including dielectric growth and metal wiring can be realized on the wafer, which effectively eliminates the problems brought by the gap to the planar process. Figure 5 shows the filling effect of the vacuum gluing process.

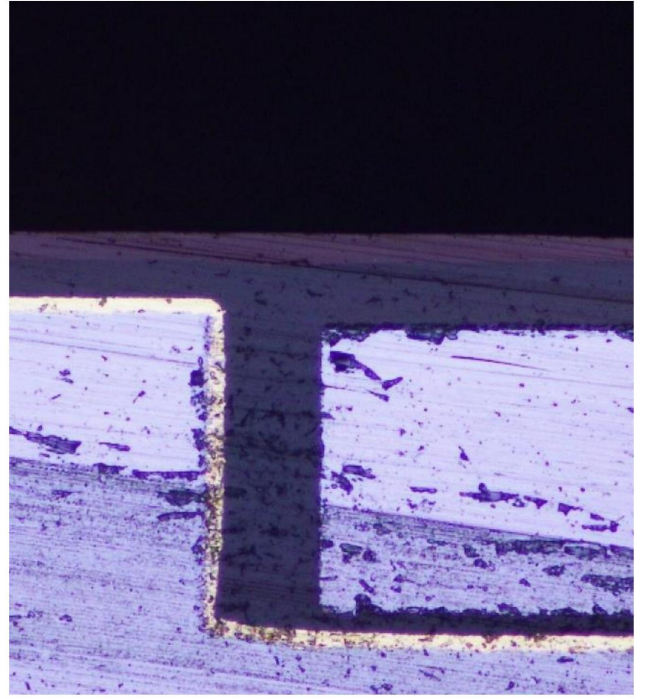


Fig. 5. cross-sectional view of vacuum gluing filling sample

III. TEST RESULTS

Fig. 6 is a silicon-based Fanout package sample of an RF chip made by the above process, and the RF performance of the sample is tested.

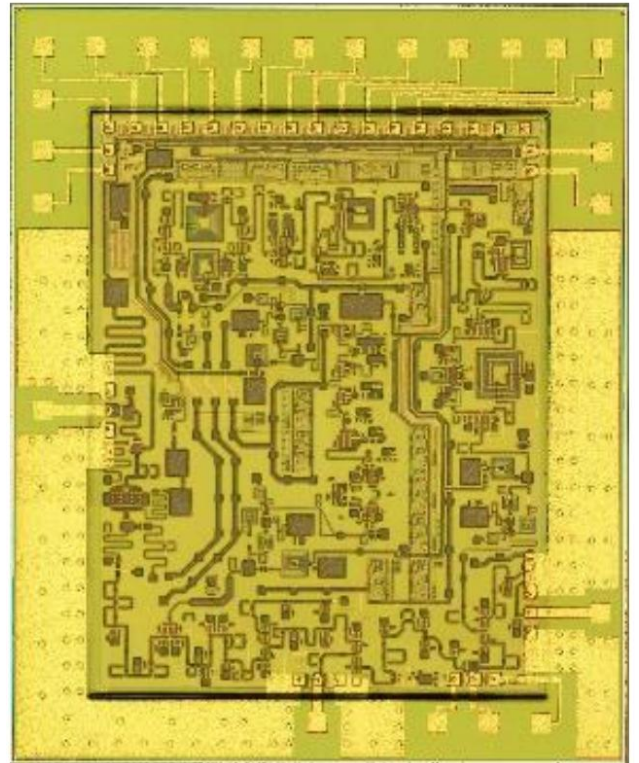


Fig. 6. silicon-based Fanout package sample

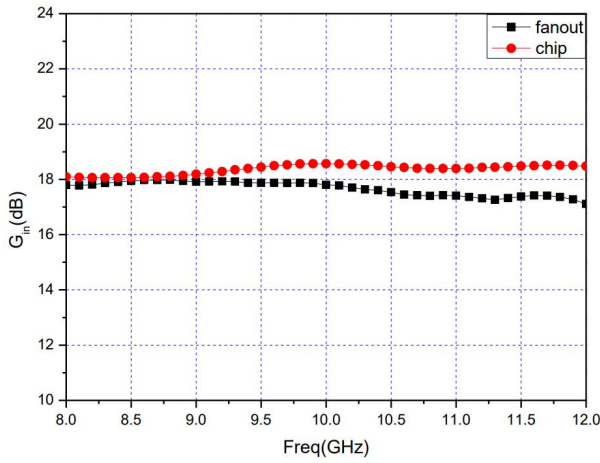


Fig. 7. emission gain

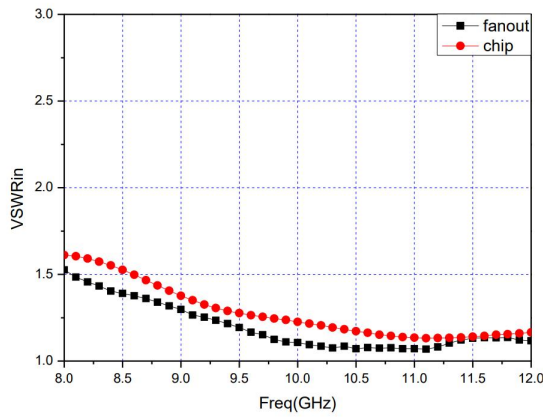


Fig. 8. emission input standing wave

The test results are shown in Figure 7 and Figure 8. The results show that the performance of RF chip packaged by silicon Fanout is equivalent to that of Die, and there is no obvious attenuation.

IV. CONCLUSION

In this paper, a silicon-based Fanout packaging technology suitable for RF chips is developed, and excellent process results and electrical test results are obtained. The results show that the silicon-based Fanout packaging technology can meet the requirements of fan-out packaging of RF chips. The key technologies include: two kinds of hole etching with different depths, copper electroplating filling and coating of passivation layer have been successfully developed, and the process flow has been confirmed, which can be applied to mass production of RF chips. This technology provides an effective solution for miniaturization, multifunction and high reliability of RF micro-systems.

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