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***Abstract*—Device miniaturization is of great concern over past two decades which leads to further transistor size shrinking and improvement in their performance. As the transistor size is reduced there is a need to include short channel effects, though these effects are not taken into consideration by conventional amplifier design (equation) based methodology.**

An alternative approach is to use graphical based Gm/Id technique. This methodology investigates the relationship between Trans conductance by drain current (gm/id) versus normalized drain current [id/ (W/L)] which is strongly related to the circuit performance. This result indicates the region of operation and also provides tool to calculate device dimensions by unified synthesis methodology in all regions of operation of a MOS transistor. In this paper, a common source amplifier with active load has been designed using Gm/Id technique to model the transistor size and meet the given design parameters such as GBW, gain and power consumption. Supply voltage of 1.8V is used here and a comparative analysis of these performance parameters is done for various technologies (180nm, 90nm, 45nm) using cadence virtuoso tool.

***Index Terms*— Gm/id technique, Short channel effects, GBW**

I. INTRODUCTION

As per the prediction of Moore's law, the number of transistors on chip have increased exponentially over past few decades while it's required to maintain low power consumption, high speed and cost reduction. In order to meet these requirements transistor sizes are reduced to a greater extent in nanometer range (current semiconductor manufacturing processes utilizes 22nm technology) for which short channel effects becomes predominant [1].

MOS modeling for transistor sizing and biasing can be done by conventional equation based technique, but it's restricted to long channel devices. An alternative approach which provides modeling of transistors including short channel effects is known as Gm/Id technique, which is based on characterization of the transistors.

Although the trend towards miniaturization has helped digital circuitry to be densely packed with transistors, the analog counterpart had to pay the price with decreasing supply voltage headroom, reduced dynamic range, lower gain, and similar other attributes [2]. As a consequence the conventional long-channel equations employed in the analog design no longer produce desired results.

In this work, a common source amplifier with active load is designed using Gm/Id technique. In section II Gm/Id technique is briefly illustrated followed by section III which describes design methodology of a common source amplifier using Gm/Id technique. Section IV provides the schematic and simulation results of the same.

II. GM/ID TECHNIQUE

Gm/Id method links design variables (Gm, ft, Id) to performance parameter (Bandwidth, power) and also employs graphs to accurately size the transistors. A methodology where transistor dimensions are obtained by fixing currents and perform complete characterization on MOS transistors to satisfy the design specifications like the gain-Bandwidth, low power, area from the derived Gm/Id ratio [3].

In long channel design, Overdrive voltage is the key parameter which determines the region of operation utilizing different set of equations where as in Gm/Id technique graphically characterize the device based on the following figure of merit.

1. Tran conductance efficiency (Gm/Id)
2. Transit frequency (ft = gm/cgg)
3. Intrinsic gain (gm/gds).

One can generate the plots with respect to these figures of merits for NMOS and PMOS characterization using cadence virtuoso tool.

III. DESIGN METHODOLOGY

In this section, a design of common source amplifier with active load is illustrated by utilizing the graphs generated from Gm/Id technique. The design specifications for this amplifier are: Unity gain bandwidth (GBW): 100MHz, slew rate (SR): 50 V/us, load capacitance (Cl): 1pF, the length is varied for 3 different technologies L = 180nm, 90nm, 45nm. The design parameters are dimensions and bias voltage of MOS Transistor.

A common source amplifier with active load is shown in fig1; here the driving MOSFET converts the variation in the input (Gate- Source) voltage into a small signal drain current (Id) which passes through the equivalent impedance of the circuit (ro1||ro2) and generates the amplified output voltage [1]. Gain of the CSA,

$$Av = - gm1 (r01||r02) \quad \ldots\ldots (1)$$

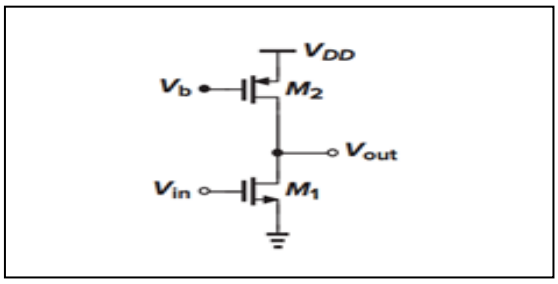

Fig1. CSA with active load [1].

i) Design of device dimension for CSA using Gm/Id technique

The design methodology is explained below step by step for NMOS device.

a) Finding the dimension (W) of NMOS Transistor

First model the NMOS transistor as shown in figure 2 obtain various plots for L = 180 nm. The Gm/Id Vs Id/W, ft vs Gm/Id, gm /gds vs gm/Id graphs are plotted by characterizing the nmos and pmos.

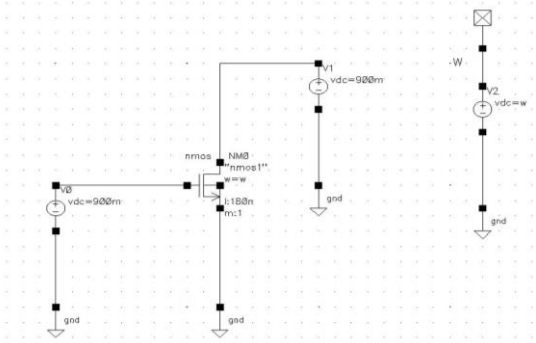

Fig2. NMOS Characterization

Secondly Gm/Id can be expressed as the ratio of the gain Bandwidth product (GBW) and the Slew rate (SR) as follows.

GBW = Gm/Cl …..(2)
SR = Id / Cl …….. (3)
From fig (i) & (ii) one can obtain
Gm/Id = GBW/SR=2*PI* 100MHz/50V = 12.6 …. (4)

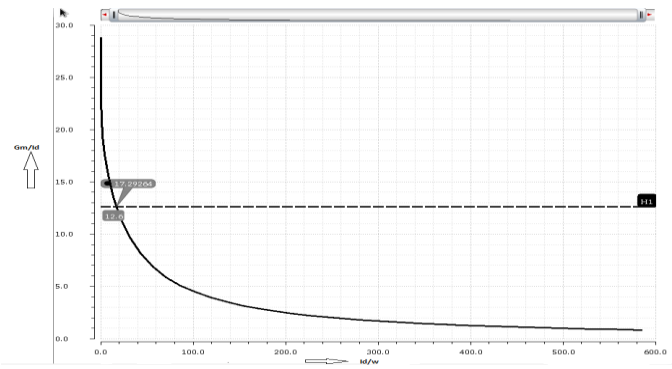

Fig3. Id/W vs Gm/Id

From figure 3 for the obtained Gm/Id value of 12.6 as in equation 4, the required Id/W is determined as 17.3.Then find out W from the obtained Id/W value as shown in equation 5.

W = Id/ (Id/W) = 50u/17.3= 3um …..(5)

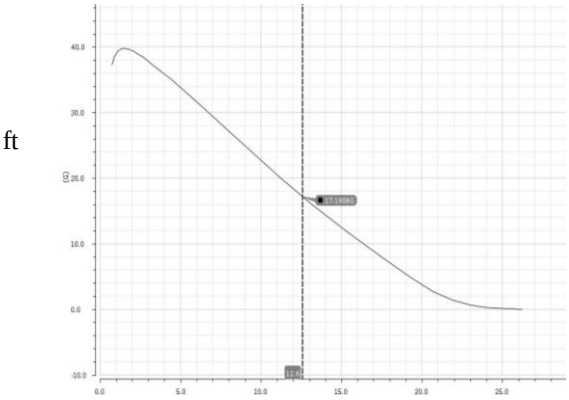

Fig4. ft vs Gm/Id

The transit frequency (ft) vs Gm/Id plot is shown in figure 4 provides useful information about the maximum speed of the device for the designed size and specified current. In order to optimize the efficiency with the speed of the circuit one need a parameter such as transit frequency ft to characterize the speed of the device [4, 6].

b) Determine the dimension of pmos transistor

The mobility of nmos is 2 to 3 times greater than that of pmos, hence. Hence the width of pmos is considered to be thrice of nmos for the same drive current [5].

ii) Finding bias voltage for *nmos /pmos* Transistor

The bias voltage for nmos /pmos transistor is obtained by Id vs Vds graph. Here one can assume maximum dynamic range. The output voltage at operating point is assumed to be mid bias voltage (0.9 Volts) by modelling the transistor as shown in figure 5. The bias voltage is determined from the nmos /pmos characteristics for the desired drain current (50 uA).

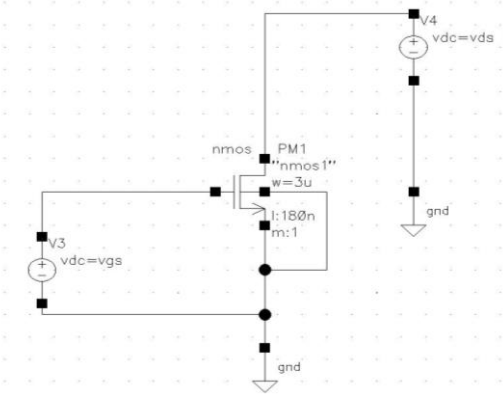

Fig5. nmos characterization

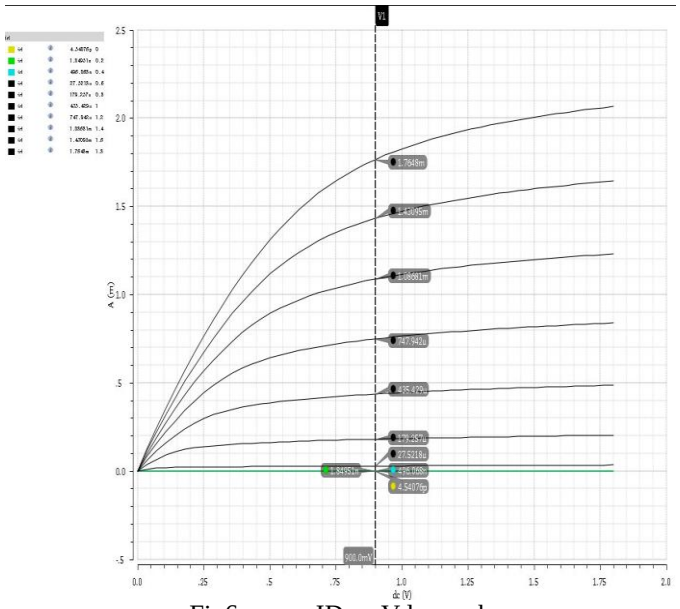

Fig6. nmos ID vs Vds graph

For the drain current of 50uA the bias voltage to be given is found to be 620mv for nmos and 1.15V for pmos to satisfy the mid biasing condition as shown in figure 6.

IV SCHEMATIC AND SIMULATION RESULTS

From the specifications, the device dimensions and the bias voltages for the CSA obtained as tabulated in table 1.

Table 1: Designed device parameters for nmos and pmos

Device	Aspect ratio	Bias Voltage
nmos	16.67	620mV
pmos	50	1.15V

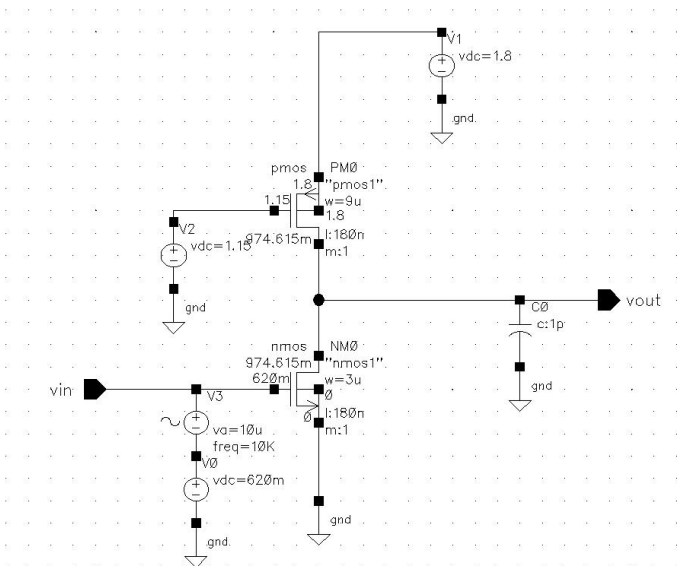

Fig7. Schematic of CSA with active load

Further DC, Transient and AC analysis was carried out to examine whether the desired specifications were met.

i) DC Analysis

The dc analysis is carried out for input voltage Vin ranging from 0 to 1.8V and graph is plotted for Vin vs Vout as shown in fig 8.

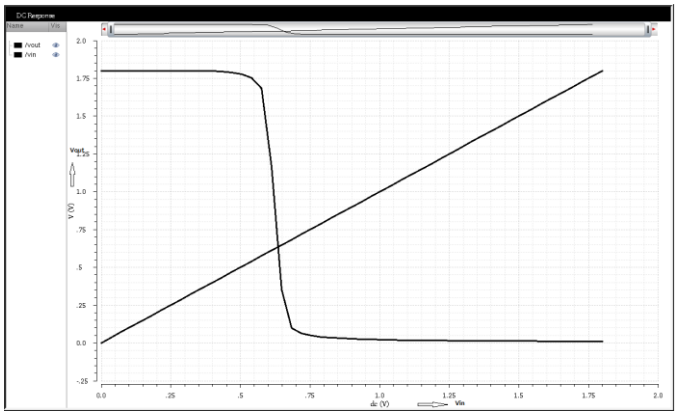

Fig 8. Plot of Transfer characteristics of CSA

Table 2: Comparison of design variables for nmos/pmos

Design variables	NMOS		PMOS
	Designed	Simulated	
gm	630us	643us	580us
id	50uA	51.19uA	-51.126uA
Gm/id	12.6	12.56	11.34
vds	900mV	974mV	-825.385mV

As shown in the table 2, the schematic analysis matches the designed specifications

ii) Transient Analysis

Transient analysis is carried out to see the input output behavior of CSA with a sinusoidal input source of 10u V, 10 KHz. An amplified output signal of gain 27d B was observed as shown in figure 9.

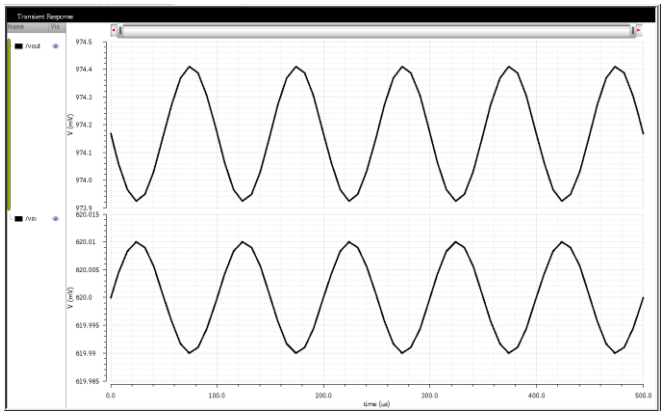

Fig 9. Input and output voltage of CSA

iii) AC Analysis

By carrying out ac analysis the frequency response graph for the circuit is generated and the unit gain Bandwidth (GBW) is noted to be 101.3MHz as shown in the fig 10.

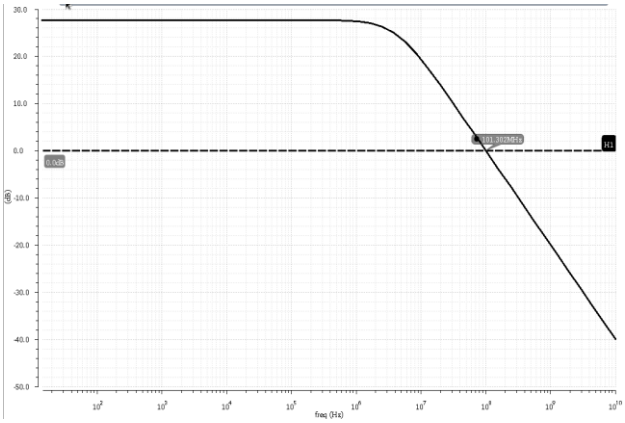

Fig 10. Frequency response graph of CSA.

Similar analysis were carried out at 90nm, 45nm technology using Gm/Id technique and it is observed that the methodology satisfies the design constraint for all the technologies(180nm,90nm,45nm) as tabulated in table 3.

Table 3: Comparison table for device parameters at various technologies

	180nm	90nm	45nm
NMOS Dimension(W)	3u	1.5u	2.5u
PMOS Dimension(W)	9u	4.5u	7.5u
GBW	101.3MHz	102.348MHz	100.8MHz
Gain	27.7dB	12.05dB	16.34dB
Power consumed	92uW	50uW	51uW

In all the technology GBW obtained is nearly 100MHz which satisfies the desired design specifications.

IV.CONCLUSION

In this work a comparative study on different technologies (180nm, 90nm, 45nm) using Gm/Id technique is been carried out to analyze the behavior of CSA for a given specification. It is observed that the specified GBW has been achieved at all technologies satisfying the requirement. Thus Gm/Id technique allows us to design the analog circuit in nanometer scale devices; hence miniaturization of transistor and meeting the required performance parameters can be achieved parallelly.

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