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Kelvin Bridge Structure Based TSV Test for Weak Faults

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***Abstract*—Due to the immaturity of manufacturing process, TSV is vulnerable to a variety of defects, which brings new testing challenges. Most of the existing test methods are suffer from the test resolution and difficult to detect weak faults. Borrowing the wisdom of Kelvin Bridge, a non-invasive test method is proposed to detect resistive open fault and leakage fault. By adjusting the resistances on the bridge arm to make them change in equal proportion, the adverse effects of contact resistance and parasitic resistance on the wire can be eliminated. HSPICE simulation using 45 nm CMOS technology show that it can successfully detect resistive open fault above 0.1 Ω and leakage fault below 10 $M\Omega$. The effectiveness of the test scheme is further proved by process-voltage-temperature (PVT) analysis.**

Keywords—Three dimensional integrated circuits (3D ICs), through silicon vias (TSVs), Kelvin Bridge, resistive open fault, leakage fault.

I. INTRODUCTION

TSVs are crucial components used for signal transmission, power supply, and fault tolerance between 3D ICs layers, but also susceptible to manufacturing defects[1]. In the manufacturing process, narrow and deep holes are first etched on the silicon wafer, then the isolation material is filled, and finally the copper is poured. Due to the imperfection of manufacturing process, defects will result in new testing challenges.

The research of TSVs testing technology is helpful to detect faults caused by physical defects in a TSV, so as to improve the yield and reliability of 3D ICs. At present, there are two kinds of representative methods in the research of TSV test: 1) probe based TSV test[2][3][4]; 2) built-in self-test (BIST) based TSV test[5][6][7].

An early method for testing TSVs directly with probes is proposed in [2]. Many single probe needle tips are utilized to contact with multiple TSVs and form a single network, which solves the problem of mismatch between TSV pitch and tip size. For a TSV with nominal value of 20 fF, the direct measurement result of probe method is 20.25 fF, which is very close to the actual value. A Micro-Electromechanical Systems based TSV probing technique is proposed to pinpoint the fault to a specific defective TSV without affecting their integrity[3]. Finite Element Analysis tool is utilized to analyze the stress on TSV pads. An efficient binary search-based algorithm is presented to guide the probe card movement and diagnose the faulty TSVs [4]. The mathematical analysis shows that the test efficiency can be greatly improved by choosing proper probe needles, and by adjusting iterative algorithm according to the fault distribution of TSVs. Generally, the advantage of the probe test method lies in its high test accuracy, but the main problem is the difficulty in test access, which is embodied in: 1) It brings additional burden to the test equipment, such as customizing and activating the probe card. 2) The probe test needs to contact the back of the wafer after thinning, which is difficult to implement in practice. 3) The contact force on the tip of TSV or solder ball may damage the TSV, resulting in the performance degradation or even failure of TSV.

A dedicated BIST test circuitry is designed to detect manufacturing defects based on charge/discharge, and sensing voltage levels at accessible end of a TSV [5]. Another BIST architecture and circuits for prebond TSV testing in 3D stacking ICs is presented in [6]. A scan switch network architecture is given to perform scan testing in test mode and operate as functional circuit in functional mode respectively. Based on the inherent RC delay characteristics of TSV, a delay based TSV test method is proposed, which maps the variation of TSV-to-substrate resistance caused by TSV defects to the change of test path delay. Recently, a BIST structure includes an improved ring oscillator to detect resistive open fault and a voltage-divider structure to detect leakage fault is presented in [7]. Compared with conventional TSV test structure, the output is more sensitive to TSV fault.

The advantage of BIST technology is that it only needs a small number of external test signals that is power/ground, clock and BIST enable signals, so the test access constraints of BIST technology are less. In addition, BIST technology does not need expensive tester or probe card, and supports test response analysis. However, most BIST technologies can only detect moderate or severe defects in a TSV, but its test accuracy is far from enough for weak open and slight leakage faults. For example, in ideal condition, TSV resistance is about 20-60 $m\Omega$, which belongs to the low resistance level. However, the resistive open fault measured by the existing BIST method is 200-1000 Ω, which is about 3000-50000 times higher than the nominal value of a TSV fault free. The fundamental reason is that, unlike probe testing, the existing BIST methods are essentially an indirect test methods. Most BIST methods use indirectly measured parameters, such as duty cycle[8][9], oscillation period of ring oscillator[10][11][12], pulse shrinkage[13][14], etc. to characterize the variation of resistance and capacitance of TSV, so as to get the severity of faults. However, the influence of additional resistance such as contact resistance and wire parasitic resistance at the contact point is ignored. For serious open fault and leakage fault, the detection effect is good, but when it comes to weak resistive open fault or slight leakage fault, the testing accuracy is far from perfect.

Motivated by this potint, based on the principle of Kelvin Bridge testing low resistance, a novel TSV test scheme based on Kelvin Bridge structure (or KB scheme for short) is proposed in this paper. Four resistors R_1, R_2, R_3 and R_4

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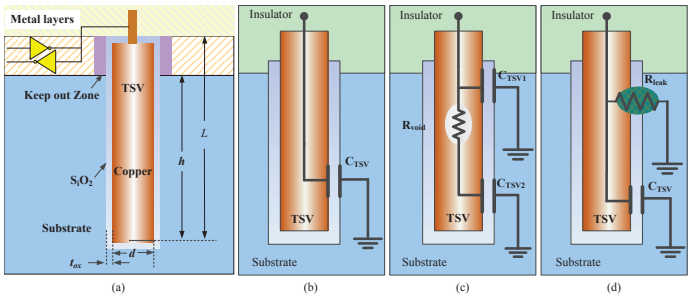

Fig. 1. Electrical model and fault model of TSV before bonding. (a) Electrical model, (b) fault free, (c) resistive open fault, (d) leakage fault.

are used to form a Kelvin bridge circuit, while R_3 and R_4 are changed in the same proportion with R_1 and R_2 respectively. When the bridge is balanced, the influence of additional resistance such as contact resistance and parasitic resistance of connecting wires can be eliminated. The technical contribution of this paper mainly includes the following aspects.

1) Compared with the probe test method, KB method draws on the advantages of BIST method and overcomes the test access problem in the probe test method. Like BIST method, KB scheme is a non-invasive test scheme, which successfully solves the problem of test access.

2) By using the characteristics of Kelvin Bridge, the adverse effect of additional resistance on test accuracy is successfully eliminated. For the measurement of median resistance, the influence of additional resistance such as contact resistance and parasitic resistance can be ignored. However, the normal resistance of a TSV is usually milliohm level, and thus additional resistance can not be ignored. In the KB method, the resistance on bridge arm is changed proportionally to remove the adverse effect of additional resistance.

3) Kelvin bridge is often used to measure the resistance value of $10^{-3} - 10^{2}\Omega$, so KB scheme can realize accurate measurement of milliohm resistance of the same level as TSVs. The proposed KB scheme can successfully detect resistive open fault above 0.1 Ω and leakage fault below 10 $M\Omega$. Compared with most BIST methods, the test accuracy is enhanced significantly.

4) Last, but not the least, PVT analysis proves the effectiveness of the proposed scheme, which enables the KB scheme more practical.

The remainder of the paper is organized as follows. Section II presents the electrical model and fault model of TSVs. The Kelvin Bridge test scheme is detailed in section III. The corresponding simulation results will be elaborated in section IV. Finally, we conclude this work in section V.

II. Electrical Model and Fault Model of TSVs

A. Electrical model of TSVs

Fig. 1 (a) shows the TSV structure before bonding. TSV can be considered as a cylindrical metal bar insolated to the silicon body by a S_iO_2 layer. Its resistance and capacitance can be calculated as[13]:

$$R_{TSV} \approx \frac{4\rho h}{\pi d^2} \tag{1}$$

$$C_{TSV} = \frac{2\pi\varepsilon h}{\ln\left[\left(d + 2t_{ox}\right)/d\right]} + \frac{\pi\varepsilon d^2}{4t_{ox}} \tag{2}$$

Here, d and h are the diameter and the height of a TSV. t_{ox} represents the thickness of isolation material S_iO_2 and is taken as 0.25 μm, ε is the dielectric constant of the isolation layer and can be taken as $8.85 * 3.9 * 10^{-3} fF/\mu m$. Due to the height and diameter of a TSV are in micron level, the copper resistivity ρ will be translated to 17.2 $m\Omega * \mu m$ after unit conversion. The aspect ratio of TSV can be taken as 15:1, i.e. h and d are 75 μm and 5 μm respectively. If the above parameters are brought into formula (1) and formula (2), and then the resistance and capacitance of TSV can be derived as $R_{TSV} = 65.73m\Omega$, $C_{TSV} = 173.27fF$ respectively.

Generally, the parasitic resistance of a TSV produced by various manufacturers ranges from several milliohms to several tens of milliohms, which is within 100 $m\Omega$. The parasitic capacitance of a TSV fluctuates from tens to hundreds of femtofarads, generally less than 1000 fF. In addition to aspect ratio, combined with other electrical parameters of a TSV, it is assumed that $R_{TSV} = 60m\Omega$ and $C_{TSV} = 200fF$.

B. Fault model of TSVs

A fault free TSV is similar to a wire and can be modeled by resistance R, capacitance C and inductance L mentioned in many literatures[8][10][15][16][17]. The defects introduced in the manufacturing process of copper pillars or sidewalls will change the electrical parameters of TSVs.

As shown in Fig. 1 (b), due to the small resistance and inductance of TSV, R and L parts are usually neglected before bonding, and only the simplified model of parasitic capacitance C between TSV and substrate is considered.

Immature TSV manufacturing process will make the TSV have micro voids defects or pinholes defects. As shown in Fig.1 (c), typical defects such as micro voids, underfilling during fabrication and misalignment during bonding will increase the resistance of TSV expressed as R_{void}. The size and position of micro voids determines the R_{void} change from zero to infinity. Ideally, $\mathrm{R}_{void} = 0$, indicating that the TSV has no fault. The worst case scenario is R_{void}=∞, which means the TSV is completely broken and modeled as a full open fault. At this time, the TSV capacitance is divided into the upper part $C_{TSV1} = x/h * C_{TSV}$ and the lower part $C_{TSV2} = (1 - x/h) * C_{TSV}$ respectively, where x represents the location of the micro void. Therefore, the position and size of micro voids will affect the contribution of part of the capacitance C_{TSV2} to the whole TSV capacitance. When there is no micro voids defect, the capacitance contribution of C_{TSV2} to TSV is 100%, and thus TSV capacitance is $C_{TSV} = C_{TSV1} + C_{TSV2}$. When the micro void increases to a certain extent, the lower part is completely isolated by micro void. Therefore, the contribution of C_{TSV2} to TSV capacitance is 0 and the TSV capacitance is $C_{TSV1} = x/h * C_{TSV}$.

Due to the impurities, incomplete deposition and mechanical stress, S_iO_2, the isolation material of TSV copper cylinder produces irregular cracks, i.e. pinhole defect. As shown in Fig. 1 (d), pinhole defect leads to a conduction path between TSV and substrate, which can be modeled as leakage fault R_{leak}. The leakage current between TSV and substrate will

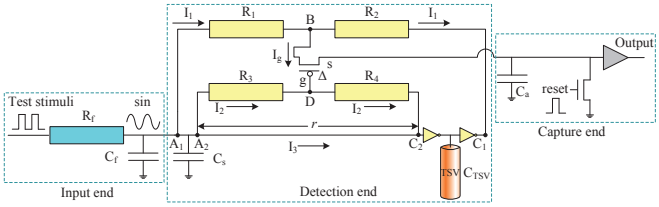

Fig. 2. TSV test structure based on Kelvin Bridge

increase significantly as pinhole defect becomes more serious. The larger the pinhole defect is, the smaller the R_{leak} is. Ideally, when there is no pinhole defect, R_{leak}=∞, there is no leakage fault.

III. TSV TEST SCHEME BASED ON KELVIN BRIDGE

A. TSV test structure based on Kelvin Bridge

The objective of this method is to test the resistive open fault and leakage fault in a TSV. Fig. 2 describes the schematic diagram of the TSV test scheme based on Kelvin Bridge, which includes three parts, that is, input end, detection end and capture end.

At the input end, the ring oscillator with five inverters is used to generate the test signal, and then the low-pass filter with filter resistor R_f and filter capacitor C_f is used to filter the test signal, and the generated pseudo sine wave is used as the AC source of Kelvin Bridge at the detection end, where $R_f = 1K\Omega$ and $C_f = 100fF$. In order to make the capacitance in the filter as small as possible, the frequency of the test signal should be relatively high. In this test structure, the ring oscillator generates a test signal with a frequency of 1GHz.

The detection end consists of four resistors: R_1, R_2, R_3 and R_4, a reference capacitor C_s, a PMOS transistor g and a TSV under test with a driver and a receiver. The contact resistance of A_1, C_1 and the parasitic resistance of wire to R_1, R_2 are respectively connected in series with R_1 and R_2 with relatively large resistance, so the influence of contact resistance and parasitic resistance of wire can be ignored. Similarly, the contact resistance of A_2, C_2 and the parasitic resistance of wire to R_3 and R_4 are incorporated into R_3 and R_4 with larger resistance. A_2 and C_2 are connected by thick wires. It can be assumed that the parasitic resistance of the wire between A_2 and C_2, and the contact resistance of A_2 and C_2 are combined together and expressed as r. Whether the contact resistance of node D is incorporated into R_3, R_4 or g, the influence on the measurement results can be ignored.

The reference capacitor C_s is implemented by a metal insulator semiconductor (MIS) capacitor. With the change of applied voltage, the capacitance of MIS structure will also change. Since the input signal oscillates around $V_{DD}/2$, the capacitance of MIS structure is in the strong inversion region most of the time. Because the capacitance of a MIS structure is always constant in the strong inversion region, for the sake of simplification, the capacitance C_s in the Kelvin Bridge is regarded as a constant.

A PMOS transistor g is utilized as a comparator, which plays the role of galvanometer. Its function is to detect whether the voltage of node B and node D at intermediate point of two bridge arms are balanced. When the Kelvin Bridge reaches the equilibrium, the voltage levels are equal at node B and node D, and the current $I_g = 0$ in galvanometer. The voltage level at the gate (V_g) and the source (V_s) of transistor g are sensed and the difference between them, that is, V_{gs} or V_{BD} is used as the criterion to determine whether the Kelvin Bridge circuit is balanced. It is worth noting that for traditional Kelvin Bridge, when the bridge circuit is balanced, the magnitude and phase of the intermediate point in two bridge arms are equal. However, in the bridge circuit in this paper, only V_{gs} is greater than or equal to the threshold voltage V_{th}, PMOS transistor g can turn on. Therefore, there should be an amplitude difference Δ between node B and node D to achieve balance.

At the capture end, the accumulation capacitor C_a is connected to the source of PMOS transistor g. When g is turned on, C_a is charged through the PMOS to realize the energy storage function. A NMOS is used to discharge C_a that is controlled by the reset signal. The reset signal is applied at the beginning of the test process to remove the charge on the accumulation capacitor C_a. The reset NMOS should be larger than the PMOS to ensure successful reset. After the reset signal becomes low, C_a will be charged or discharged if the TSV has defects.

B. Testing principle of Kelvin Bridge

As shown in Fig. 2, the current passing through R_1 and R_2 is equal, which is represented by I_1. Similarly, the current through R_3 and R_4 are equal, expressed as I_2. The current through TSV and C_s are also equal, expressed as I_3. When the Kelvin Bridge is balanced, the current I_g in the PMOS will be 0 and the voltage level of B and D are equal. According to Kirchhoff law, the following equations will hold.

$$I_3 R_{TSV} + I_2 R_3 = I_1 R_1 \tag{3}$$

$$I_3 R_s + I_2 R_4 = I_1 R_2 \tag{4}$$

$$I_2(R_3 + R_4) = (I_3 - I_2)r \tag{5}$$

Formula (6) can be obtained by the combination of formula (3), (4) and (5).

$$R_{TSV} = \frac{R_1}{R_2} R_s + \frac{R_4 r}{R_3 + R_4 + r}\left(\frac{R_1}{R_2} - \frac{R_3}{R_4}\right) \tag{6}$$

It can be seen from formula (6) that the additional resistance r exists in the correction term of the second part in formula (6). Suppose $\frac{R_1}{R_2} = \frac{R_3}{R_4}$ is true, and then the correction term will be always equal to zero, and formula (6) will be transformed into $R_{TSV} = \frac{R_1}{R_2} R_s$. It can be concluded that under the condition that R_3 and R_4 change with R_1 and R_2 in the same proportion respectively, when the bridge is balanced, the adverse effect of additional resistance r can be eliminated, and the accurate measurement of TSV electrical parameters can be achieved.

Considering that the galvanometer is realized by a PMOS and the PMOS has a threshold voltage V_{th}, formula (7) can be deduced.

$$\Delta + \frac{R_{TSV}}{R_1 + R_{TSV}} = \frac{R_s}{R_2 + R_s} \tag{7}$$

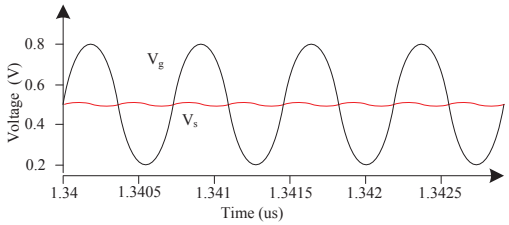

Fig. 3. Voltage waveform of the gate V_g and the source V_s on the PMOS transistor g

In addition, in the case of AC power supply, formula (7) is equivalent to the following formula (8).

$$\Delta + \frac{\frac{1}{j\omega C_{TSV}}}{R_1 + \frac{1}{j\omega C_{TSV}}} = \frac{\frac{1}{j\omega C_s}}{R_2 + \frac{1}{j\omega C_s}} \tag{8}$$

Here, Δ=$\mathrm{V_{th}}/\mathrm{V_{DD}}$, C_s is the reference capacitance, R_{TSV} and C_{TSV} are the resistance and capacitance of the TSV to be tested respectively.

It can be seen from the equation above that Δ is a complex number, but we only need to consider the real part of Δ, not the imaginary part, since the phase difference between the two arms is very small. Due to voltage difference Δ, the resistor and capacitor of the two arms is different from that of the general AC bridges. If the bridge circuit is unbalanced, for example, the voltage difference is larger than Δ, the PMOS will be turned on.

Assuming that the TSV capacitance is 60 fF, the voltage waveforms of the gate V_g and the source V_s on the PMOS transistor g are shown in Fig. 3 to illustrate the operation process of the Kelvin Bridge. When V_g is less than V_s and the voltage difference reaches V_{th}, the PMOS g will be turned on and thus C_a is connected to the source node.

At the capture end, the C_a is used as an accumulator and is set to 50 fF. When the voltage passing through C_a is higher than the threshold value of the connected buffer, the output will be flipped from low level to high level.

IV. Simulation Results and Analysis

In order to evaluate the performance, detection range, and robustness against PVT of proposed KB method, HSPICE is used to simulate in 45 nm process. The process model uses 45 nm PTM CMOS process[18][19], and the reference voltage V_{DD} is 1.1 V. In the simulation, it is assumed that resistive open fault occurs in the middle of TSV. The detailed parameters used in the test structure are listed in Table I. The appropriate method to select the bridge arm resistance will be introduced later in this section. For the sake of simplification, the parasitic resistance and capacitance of TSV are assumed to be 60 $m\Omega$ and 200 fF respectively.

A. Test resolution of resistive open fault

In this section, a PMOS g in Fig. 2 is used as a comparator to detect whether the intermediate points B and D of the two bridge arms are balanced. The voltage level at the gate (V_g) and source (V_s) of PMOS g are sensed, and the difference between them is used as the criterion to determine whether the Kelvin Bridge is balanced, so as to characterize the resistive

TABLE I. Parameters used in KB test structure

Symbol	Value	Tolerance	Position
R_f	$1K\Omega$	0, 10%	Input end
C_f	$100fF$	0, 10%	Input end
R_1	60Ω	0, 10%	Detection end
R_2	$60K\Omega$	0, 10%	Detection end
R_3	20Ω	0, 10%	Detection end
R_4	$20K\Omega$	0, 10%	Detection end
C_s	$200fF$	0, 10%	Detection end
R_{TSV}	$60m\Omega$		Detection end
C_{TSV}	$200fF$		Detection end
C_a	$50fF$	0, 10%	Capture end

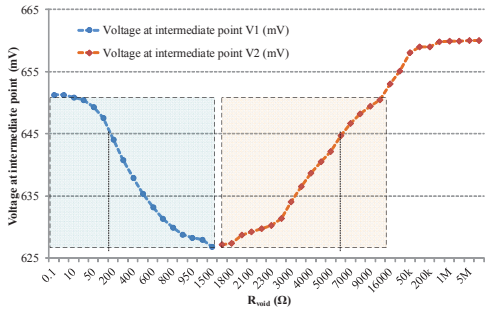

Fig. 4. Characteristic curve of voltage at intermediate point under resistive open fault

open fault and leakage fault in a TSV. Assuming that the initial state of Kelvin Bridge is in the state of equilibrium, the measured voltage of V_{BD} is 651.263 mV. After injecting resistive open fault or leakage fault into TSV, the slight fluctuation of voltage V_{BD} at equilibrium point can be utilized to detect the fault. Fig. 4 depicts the characteristic curve of voltage at intermediate point under resistive open fault. In general, the characteristic curve can be divided into left and right parts, which are drawn in blue and orange, and represented by V_1 and V_2 respectively.

In the right part, when the range of R_{void} is in the interval $[1500\Omega, 1M\Omega]$, the value of V_2 gradually increased from 626.886 mV to 659.875 mV, showing an obvious increasing trend with R_{void}. When the range of R_{void} lies in the range of $[1M\Omega, 5M\Omega]$, the value of V_2 is in the interval $[659.875mV, 659.963mV]$. At this time, the growth rate of V_2 is relatively gentle, close to the saturation state, and the intermediate point voltage basically does not continue to increase. Combined with the electrical model of resistive open fault, when R_{void} increases to $1M\Omega$, it can be considered that TSV has completely broken at the position $h/2$.

In the left half, as R_{void} decrease gradually from 1500 Ω to 0.1 Ω, the value of increased from 626.886 mV to 651.262 mV. In particular, the value of V_1 remains constant at 651.262 mV when R_{void} is 0.1 Ω, which is very close to the intermediate point voltage in the balanced state. This shows that as the R_{void} becomes smaller and smaller, the TSV tends to be in the ideal fault free state. TSV can be treated as fault free when $R_{void} = 0.1\Omega$, which is the weakest resistive open fault that KB scheme can detect.

The existing BIST schemes are usually easier to detect medium or severe resistive open faults. However, the resistive open faults with lower R_{void} are usually more difficult to detect. Therefore, the minimum value of R_{void} that can be detected is usually one of the important reference criteria to evaluate a BIST Scheme. As far as we know, it has been

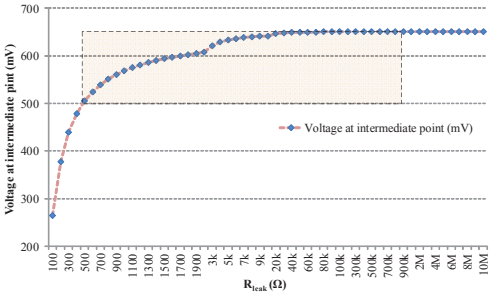

Fig. 5. Characteristic curve of voltage at intermediate point under leakage fault

reported in literature that the minimum resistive open fault can be detected is $200\Omega - 1K\Omega$ or even higher[8][13][17]. Benefit from the excellent detection capability of Kelvin Bridge for small and medium resistance, the KB scheme in this paper is obviously superior to most known BIST schemes.

It should be noted that from Fig. 4, it can be found that one intermediate point voltage corresponds to two R_{void} in the partial detectable region $0.1\Omega - 1M\Omega$, which will cause test confusion. For example, $V_1 = V_2 = 645mV$ under the condition of $R_{void} = 200\Omega$ or $R_{void} = 6K\Omega$. In other words, when the intermediate point voltage is detected to be 645 mV, it is difficult to distinguish the resistive open fault with 200 Ω or 6 $K\Omega$ in a TSV to be tested. This situation can be explained from the perspective of the electrical model of the resistive open fault. Under mild resistive open fault, such as less than 1500 Ω, R_{void} has little contribution to the voltage at intermediate point, but C_{TSV} remains basically unchanged and plays a dominant role. However, as R_{void} increases gradually, especially when $R_{void} = 1M\Omega$, which indicates that the TSV is completely broken. At this time, C_{TSV} is reduced to half of the original, that is 100 fF, and the contribution of R_{void} to the voltage at intermediate point is increased. In practice, the test process needs to be designed reasonably, and it often requires multiple rounds of testing to completely remove the faults in a TSV. Therefore, in the process of test practice, the existing BIST method can be used to conduct a preliminary test to remove the resistive open fault with R_{void} more than 1500 Ω. This step is equivalent to excluding the right half of Fig. 4, and then using the KB scheme in this paper, the fault characteristics of R_{void} from 0.1 Ω to 1500 Ω can be detected. Therefore, the KB method is particularly suitable for the detection of weak open fault.

B. Test resolution of leakage fault

Fig. 5 shows the characteristic curve of the voltage at intermediate point under leakage fault. It can be found that as the equivalent resistance of leakage fault R_{leak} increases from 100 Ω to 10 $M\Omega$, the voltage at intermediate point increases from 264.954 mV to 651.256 mV. This can be explained in two aspects. On one hand, under the condition of $R_{leak} < 100\Omega$, V_{BD} will be less than 264.954 mV, galvanometer g fails to conduct, and C_a cannot be charged or discharged. On the other hand, when R_{leak} increases from 1 $M\Omega$ to 10 $M\Omega$, although V_{BD} also increases gradually, it tends to be placid. This shows that when $R_{leak} \geq 1M\Omega$, the equivalent resistance of leakage fault is large and the leakage current is very small, which can be considered as approaching the fault free state. Therefore, in the KB method, the detection range of leakage fault is $[100\Omega, 10M\Omega]$, and the preferred detection range is $[100\Omega, 1M\Omega]$ as shown in the rectangle in Fig. 5.

Through the above analysis, it can be summarized that there are three differences between leakage fault and resistive open fault. Firstly, leakage fault will not be affected by TSV parasitic capacitance as resistive open fault. Therefore, the characteristic curve of leakage fault is a rising curve, which will not be divided into two parts as shown in Fig. 4. Secondly, different from the resistive open fault, the smaller the R_{void} is, the more difficult it is to detect. The larger the equivalent resistance R_{leak}, the more difficult it is to detect in terms of leakage fault. Leakage fault with $R_{leak} < 10K\Omega$ is usually considered to be serious leakage fault, which can be detected by conventional methods in the preliminary detection. The equivalent leakage current of $R_{leak} = 10M\Omega$ is 0.1 μA. It can also be concluded that KB method can detect such a very weak leakage fault as the minimum of 0.1 μA, which is better than most existing test methods. At last, compared with the V_{BD} (651.263 mV) of fault free, resistive open fault will increase the V_{BD}, while leakage fault will decrease V_{BD}, which is the opposite. Assuming that there is only one type of fault, the KB method can successfully distinguish the resistive open fault from the leakage fault according to the voltage V_{BD} at intermediate point.

In a word, the minimum value of resistive open fault detected by KB method can be achieved by 0.1 Ω, and the measured resistance R_{void} is very close to the nominal resistance $R_{TSV} = 60m\Omega$ of fault free. Furthermore, the KB method can detect a weak leakage fault such as 10 $M\Omega$.Therefore, from the view of test accuracy and detection range, KB method is a test method with excellent performance. However, each coin has two sides. The KB method cannot detect serious resistive open fault very well, or KB method alone will cause some degree of test confusion in terms of resistive open fault, which is inferior to the existing methods, but can be solved by properly design in the test process. This is also make sense as we usually use cursor calipers to achieve 0.01 millimeter-level accuracy, however, it is not appropriate to use them to measure objects of meter-level length.

C. The Effect of PVT on the Kelvin Bridge

In order to verify the applicability and robustness of KB method, the influence of process variation, voltage and temperature (PVT) of the method is discussed in this section. It is assumed that the fluctuation of resistance and capacitance used in bridge arm is $\pm 10\%$. The supply voltage is 0.9 V, 1 V and 1.1 V respectively, and the temperature environment is $0°C$, $25°C$ and $105°C$ respectively. Given the supply voltage of 1 V, temperature T= 25 $°C$, comparison of voltage at intermediate point under resistive open fault and leakage fault is depicted in Fig. 6. Here, different values of R and C represent different process corners. For example, $(0.9R, 1.1C)$ means that the resistance and capacitance are 0.9 and 1.1 times of the standard value respectively. Absolute deviation (AD) is defined as the absolute value of voltage between process corner and standard corner. Relative deviation (RD) is defined as the average ratio of the voltage at intermediate point between the simulation corner and the standard corner.

As shown in Fig. 6, it can be found that both resistive open fault and leakage fault have the minimum RD under process

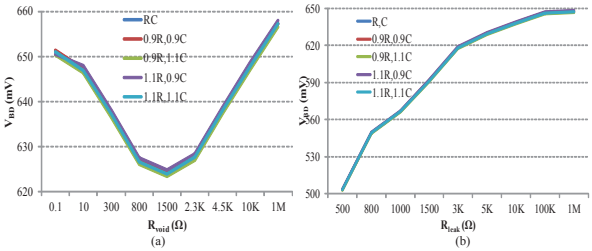

Fig. 6. The voltage distribution at intermediate point under various process corners. (a) Variation of voltage at intermediate point under resistive open fault. (b) Variation of voltage at intermediate point under leakage fault.

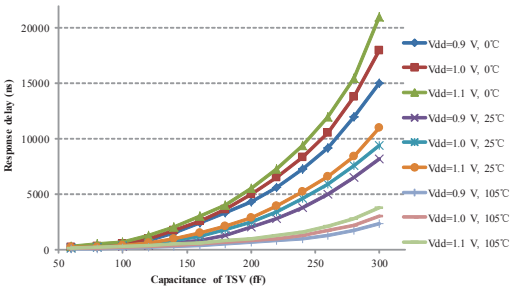

Fig. 7. Response delay of KB test architecture under different PVT corners.

corner $(0.9R, 0.9C)$ and the maximum RD under process corner $(0.9R, 1.1C)$. It can be concluded that TSV capacitance has more influence on process variation. In addition, it should be noted that in each process corner, with the increase of R_{leak}, the AD shows an increasing trend, which is different from R_{void}. In general, the KB test method proposed in this paper has a good adaptability in all process corners, and is not sensitive to the variation of resistance and capacitance.

Fig. 7 shows the relationship between the TSV capacitance and the response delay of KB test circuit at various PVT corners. It can be seen that the overall distribution of response delay presents an obvious three beam curve at $0°C$, $25°C$ and $105°C$. On the contrary, the curves fluctuate little under the same temperature and different supply voltage. After calculation, the range of output delay fluctuation is $\pm 3\%$. In addition, the longest response delay can be found at (1.1V, $0°C$). It can be concluded that the temperature deviation has more influence on the response delay than the supply voltage deviation.

V. Conclusion

Different from the serious fault, the weak fault is usually more difficult to be detected, which will leave a hidden danger to the later process, yield and reliability. Conversely, higher test accuracy can reduce the escape rate of failure, which is conducive to improve the yield and product quality of 3D ICs. The test structure based on Kelvin Bridge proposed in this paper can detect the resistive open fault of 0.1 Ω level successfully, which is very close to the ideal fault free. In addition, it can detect 10 $M\Omega$ leakage fault, which is equivalent to 0.1 μA leakage current, while PVT analysis proves the effectiveness of the proposed scheme.

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