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Bi-Directional Time Domain Duplexing (TDD) Amplifier for 5G Applications

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***Abstract*— In Time Division Duplex Systems (TDD) the transmitter and receiver are not ON simultaneously. This is done to avoid the saturation of the receiver's LNA from the high power that can get leaked into the receiver due to limited isolation. Since, either the PA or the LNA is working at a given instant of time, the area and power can be saved by designing a circuit that can work as LNA or PA at different instances in time. Low power and reduced Si area leads to reliability and cost reduction. This work presents the design of a bi-directional amplifier (BDA) in sub 5GHz range. The design contains a two-stage inductor-less LNA along with transistor-based switches and 50Ω drivers for off-chip testing. The design is implemented in Skywater 130nm CMOS open-source PDK. The results show 25.55dB voltage gain in reception mode (without buffer), less than 3.5dB noise figure in 1-4.5GHz band with input matching of -10dB. The power consumption of the proposed design is 58mW with active chip area 204x166µm^2.**

***Keywords*— Bi-Directional Amplifier, LNA, Wideband LNA, 5G LNA, 130nm CMOS, Open Source, Inductorless LNA**

I. Introduction

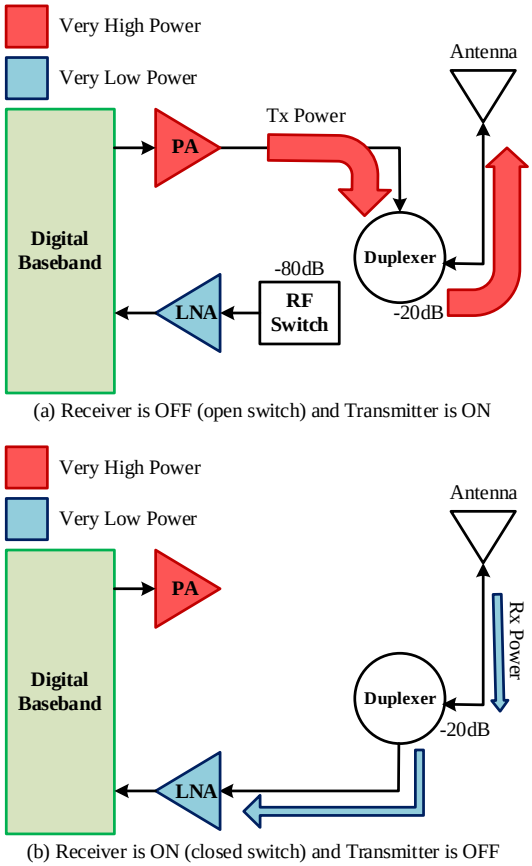
Classical transceiver architectures are half-duplex in nature. The data is divided either in time or frequency domain. The receiver and transmitter chains that share the same antenna at the RF front ends are never turned ON simultaneously [1]. At a given instance of time, either the transmitter or the receiver is working. During the transmission, the receiver chain is isolated through an RF switch (80~100 dB isolation) as shown in Fig. 1. This is done because the power at the end of the transmitter chain (output of power amplifier) can be billions of times (~100dB) larger than the intended received power. If the receiver is ON during transmission, the leaked power from the transmitter can easily saturate the low noise amplifier of the receiver; rendering the transceiver useless. Therefore, the transmission and reception are time duplexed [2].

Low noise amplification circuit with a high voltage gain, high linearity, and wide band input matching with low power consumption is a very challenging design problem [3]. Different circuit topologies with different characteristics are combined to improve different design parameters in order to reach an optimum circuit that satisfies the specifications for a given application [4]. Common source cascode amplifier with inductive degeneration and shunt peaking is a classical circuit extensively used in low noise amplifier designs for narrow band applications [5]. Although the cascode LNA with inductive degeneration provides a good noise and gain performance, but its input matching is very narrow band. To increase the bandwidth, common gate topology can be utilized [6]. The input impedance is matched using the transconductance of the input transistor. This topology does not suffer from the miller capacitance, however a cascode is employed to isolate the input and output impedance and to increase the output resistance for maximum voltage gain.

The design shown in Fig. 2 employs multiple techniques like current reuse, self-bias, and resistive feedback to achieve low noise operation in the 0.1-1.2 GHz band [7]. The transistors M1a and M1b are connected with resistance R_f. This is a type of trans-impedance amplifier. R_1 and C_1 form a high pass filter that blocks the flicker noise, but passes the channel thermal noise. Transistor M2 and M3 are biased such that they cancel the noise of the transistors M1a and M1b.

Similarly, another inductor less wideband differential LNA is presented by [8], for 1-7 GHz band. It utilizes current re-use, voltage to current feedback, and cascode configuration to achieve the low noise amplification operation along with high gain and wide input matching. It also utilizes techniques of optimum biasing to improve the linearity of the given LNA architecture [9].

Since RF front end is inherently time duplexed in nature, hence this characteristic can be exploited to design a single circuit that can act as both LNA and PA, instead of separate transmitter and receiver amplifiers [10]. This makes sense as



(a) Receiver is OFF (open switch) and Transmitter is ON

(b) Receiver is ON (closed switch) and Transmitter is OFF

Fig. 1. Classical transceiver architecture with shared antenna during transmission

only LNA or PA is working at a given time. A single circuit that can perform both functionalities will not only reduce power but also on-chip area. Power reduction will lead to a longer duration of operation in applications where the supply is provided by batteries. Reduction in the area directly relates to reduced cost [11]. This bi-directional scheme is more useful for WLAN Applications in sub-6 GHz domain because power required at the output of the power amplifiers in WLAN transceivers is not very high.

Rest of the paper is organized as follows. In section-II, different state-of-the-art topologies of bi-directional amplifiers are reviewed. Section-III presents the proposed circuit/architecture of the bi-directional amplifier. The implementation and results for the proposed amplifier are discussed in section-IV, followed by section-V, in which performance comparison with state-of-the-art designs is provided. The last section-VI concludes the paper.

II. State-of-the-art Bi-Directional Amplifiers

A CMOS based differential bi-directional amplifier for 5G NR applications is presented in [12]. This bi-directional amplifier is part of a complete bi-directional beam former. In this circuit, the bi-directional amplification operation is achieved in three stages. The first stage is the driver stage to drive the phase shifter port of the beam former circuit. The second is the PA-LNA stage and the third is the differential to single-ended conversion stage to drive the antenna. The schematic of the circuit is shown in Fig. 3. The first stage is a driver circuit that delivers current to the PS (phase shifter) port when the bi-directional amplifier is in LNA mode as shown in Fig. 4. A signal from the single-ended antenna is converted to differential through a balun and then the second stage, along with the driver stage, delivers this signal to the differential phase shifter port. While, in PA mode, the state of the driver and second stage is shown in Fig. 5. The signal from the PS port is amplified by both of these stages and then it is converted from the differential to single-ended through a balun again and fed to the antenna.

Likewise, [13] presented a switchless CMOS bi-directional distributed gain amplifier with multi-octave bandwidth. This amplifier architecture removes the requirement of any passive or active switches in the architecture. The schematic of the circuit is shown in Fig. 6. This amplifier is arranged in a distributed manner such that the mathematical expression for characteristic impedance (Z_o) is given in (1). Due to this distributive arrangement and setting characteristic impedance (Z_o) equal to 50Ω, this circuit achieves a very wideband matching response from 3-20 GHz. At a given instant, out of the four transistors (M1-M4) in each section, only two are ON. For example, during signal propagation from P1 to P2, transistors M1 and M2 are ON while transistors M3 and M4 are cutoff and vice versa.

$$Z_o = \sqrt{\frac{L_G}{C_{gs1}}} = \sqrt{\frac{L_D}{C_{GS4}}} = 50\Omega \qquad (1)$$

The main bottleneck of both the above mentioned designs is the presence of inductor along with distributed network of multiple amplilifiers. Both of these factors contribute significantly towards high Silicon footprint.

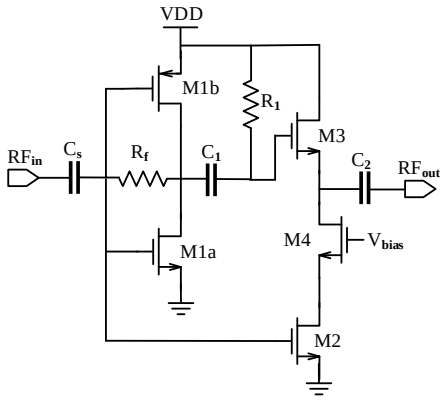


Fig. 2. Inductor less LNA Architecture [7]

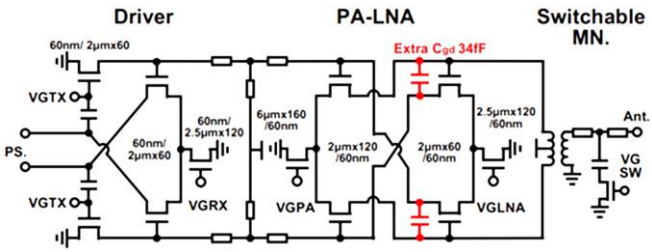


Fig. 3. CMOS based differential bi-directional amplifier for 5G NR applications [12]

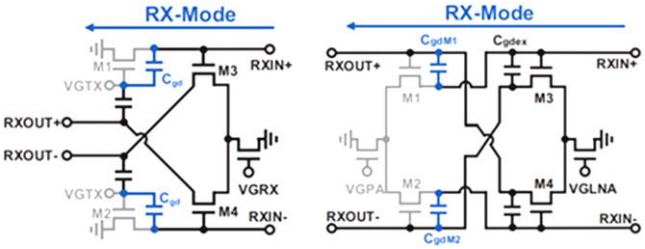


Fig. 4. State of driver and second stage in LNA mode [12]

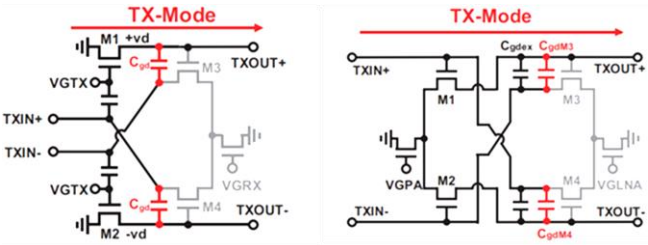


Fig. 5. State of driver and second stage in PA mode [12]

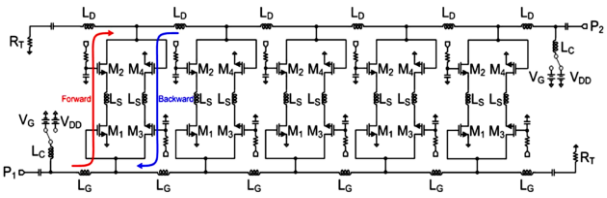


Fig. 6. Distributed Bi-Directional Amplifier [13]

III. Proposed Bi-Directional Amplifier Design

This section would discuss the architecture and design of the proposed bi-directional amplifier design for TDD (Time Domain Duplexing) systems in the Sub 6- GHz 5G band. The proposed design of BDA is highly suitable for on chip implementation because of no requirement of on-chip inductor. The implementation of proposed design in opensource SkyWater PDK is also an added advantage

fostering the development of open source IC design arena.

A. *Prooposed Architecture*

The block diagram of the proposed architecture is shown in Fig. 7, which contains an antenna that is shared in both transmission and reception. A 3-port device known as the circulator connects the antenna in such a way that it can receive the signal from one port during the reception and feed the antenna through the third port during transmission. During both transmission and reception, the amplification is provided by the "Amplifier" block. A 50Ω driver is used to drive the antenna through the circulator. The bi-directional mechanism is obtained through the use of 3 switches marked S1, S2, and S3. All of these switches are duplexed between two available paths. Antenna and circulator will be implemented through off-chip components on the PCB while the amplifier and 50Ω driver will be implemented on-chip.

1) *Transmission Mechanism*

During transmission, switch S1 is ON in such a way that it rejects the incoming signal from the antenna through the circulator while transmits the signal coming from the baseband for power amplification. Similarly, the switch S2 isolates the receiver's baseband path and transmits the voltage amplified signal from the amplifier block to the 50Ω driver. The 50Ω driver delivers power to the antenna through the circulator for wireless transmission.

2) *Reception Mechanism*

During the reception, switch S1 isolates the signal from the transmitter baseband and connects the input of the amplifier block to the circulator's port. The received signal from the antenna now comes directly to the input of the amplifier. After low noise voltage amplification, this signal goes to the receiver path where it can be down-converted and demodulated. The switch S2 disconnects the path to the 50Ω driver and S3 terminates the third port of the circulator so that no signal goes to the antenna from the 50Ω driver.

Hence, bi-directional amplification is obtained by a single amplifier block. The front-end amplifier acts as the low noise amplifier (LNA) during the reception and as the pre-driver for the power amplifier during the transmission. The mode of operation is determined by the state of the switches.

B. *Power Budget Analysis*

Since the target application for this circuit is sub 6 GHz 5G WLAN application, the system level specifications can be derived from the WLAN standard. For the Bi-Directional Amplifier Architecture, the minimum power at the receiver is >= -80dBm, and power delivered to the antenna should be <=30dBm. Typically, the transmitted power by the WLAN is around 10dBm.

Fig. 8 shows the transmission budget for the bi-directional amplifier. The amplifier and 50Ω driver then should provide a gain of 30dB for the output power to be 10 dBm. Likewise, Fig. 9 shows the reception budget for the bi-directional amplifier, where, if the amplifier provides the gain of 30 dB then the signal at the output will be -50dBm. This output is sufficient to be down-converted to baseband using the mixer and further amplification can be done in the baseband.

Along with the high gain, the amplifier should also add minimum noise to the signal i.e. it should be <=4dB in the entire band.

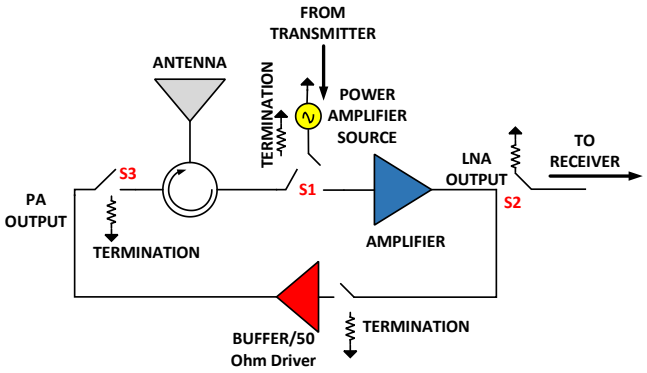


Fig. 7. Block Diagram of the proposed Bi-Directional Amplifier

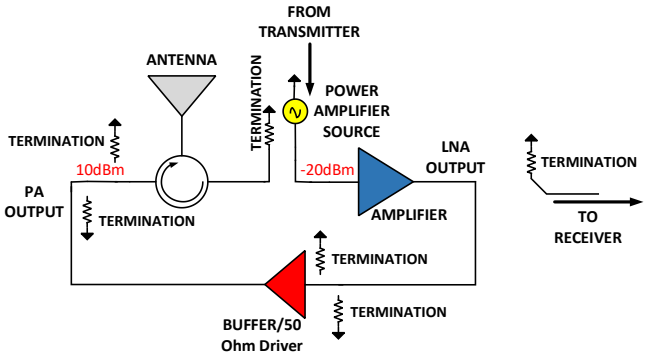


Fig. 8. Transmission power budget analysis

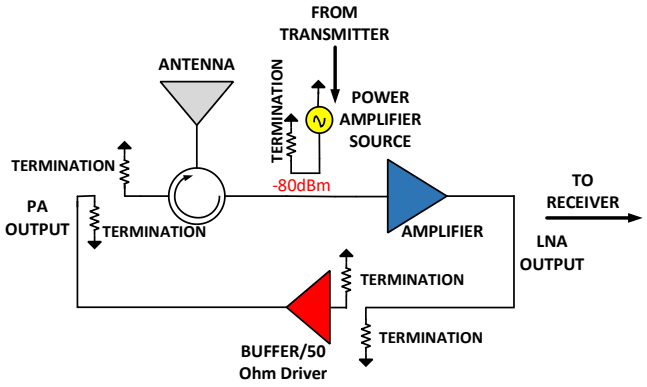


Fig. 9. Reception power budget analysis

C. *Amplifier Topology*

To minimize the area, maximize the bandwidth, and input matching, an inductor less topology is required for this design. To simultaneously provide high gain, low noise, and wide band input matching, the proposed amplifier design has two stages as presented in Fig. 10.

1) *Gain Analysis of Amplification Stage*

The first stage is main amplification stage. The mathematical expression for gain by applying small-signal analysis at differential nodes (V_{o_+}) and ($V_{o\_}$) is given in (2) and (3)(3)(3) respectively. Here, (3) is very interesting i.e. the gain at node ($V_{o\_}$) which would typically have been $g_{m4}R_0$ (common gate gain) is boosted by the factor $(1 + |A_+|)$. This means that the larger the forward voltage gain A_+, larger will be the gain at the ($V_{o\_}$) node. So, by using less power in the transistor M4, more gain is achieved.

$$A_+ \cong -(g_{m0} + g_{m1}) * R1 \qquad (2)$$

$$A_{-} = \frac{Vo_{-}}{V_{RFin}} = g_{m4} * R_0 * (1 + |A_{+}|) \quad (3)$$

2) Input Matching

The mathematical expression for the input matching can also be similarly derived from the small-signal model, which is given in (4). Due to the g_m boosting action of the forward amplifier, the transconductance required to match to the 50Ω impedance is reduced by the factor of $1 + |A_{+}|$. For the classical common gate amplifier, the transconductance required for input matching to 50Ω is 20mS. However, for this particular amplifier configuration if the forward gain A_{+} is 9, then the transconductance required to match to 50Ω impedance is $\frac{50mS}{1+9} = 5mS$. This will reduce the power and size along with input capacitance C_{gs} of the transistor M4.

$$Z_{in} = \frac{1}{g_{m4}(|A_{+}| + 1)} \quad (4)$$

3) Noise Analysis

To calculate the input-referred noise, the circuit can be simplified as shown in Fig. 11 The transistors M0-M2 have been merged into one single transistor M0 for the sake of simplicity, while resistance (R_s) is the source termination impedance i.e. 50Ω. Two currents flow through the resistor (R_1) to produce noise voltage V_{n1}. One of the currents is the channel thermal noise current of the transistor (M0) while the other current flows due to voltage V_s and the transconductance of the transistor (M0). The mathematical expression for squared input-referred noise voltage of the transistors M0-M2 is given in (5). The important observation from this expression is that the input-referred noise of the circuit can be reduced by two methods. Firstly by increasing the forward transconductance g_{m0} or secondly by increasing the forward voltage gain $|A_{+}|$. Under the limiting condition that forward voltage gain is very large i.e.$A_{+} \gg 1$, then (5) can be writtent as $V_s^2 = \frac{KT\gamma}{g_{m0}}$.

$$V_s^2 = \frac{KT\gamma}{g_{m0}\left(1 + \frac{1}{(|A_{+}|)^2}\right)} \quad (5)$$

This squared input-referred voltage noise is 4 times (6 dB) less than the input-referred noise of the typical common source amplifier which is $V_i^2 = 4 * \frac{KT\gamma}{g_m}$. So, we can see that this amplifier by design reduces the noise by 6 dB due to feedback under the impedance match condition.

The noise contribution of transistor M4 at the node ($V_{n_{+}}$) and ($V_{n_{-}}$) under input matching condition is given in (6) and (7) respectively. As the noise appears in phase at both nodes, hence the noise contribution of the transistor M4 can be, in theory, completely canceled by designing a suitable feedforward stage. This feedforward stage is the second stage of the amplifier in the Bi-directional TDD amplifier architecture as shown in Fig. 10.

$$V_{n_{-}} = -\frac{1}{2} I_{n4} R_0 \quad (6)$$

$$V_{n_{+}} = -|A_{+}| * I_{n4} * \frac{R_s}{2} \quad (7)$$

4) Overall Gain and Bandwidth Analysis

Fig. 10 graphically depicts how signal from the differential ends is added on the output node while the noise of the

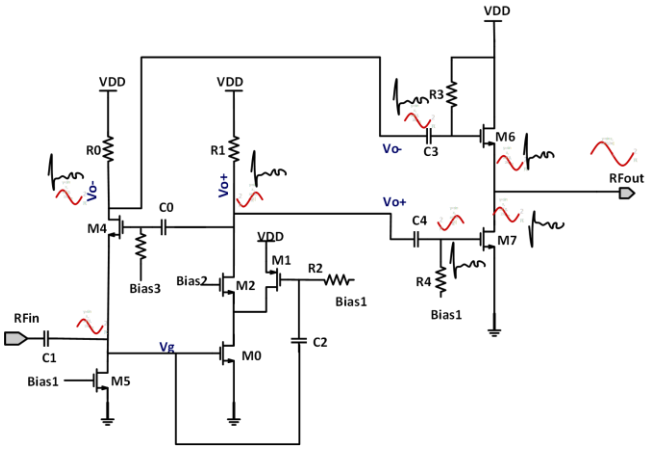


Fig. 10 Complete schematic of amplifier to be used in the bi-directional TDD architecture

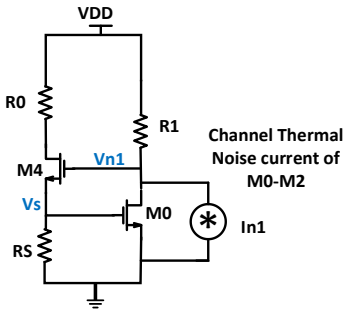


Fig. 11. Simplified circuit to calculate input-referred noise

transistor M4 is canceled at the same node. The mathematical expression for overall gain of the two-stage amplifier under input matched and the noise cancellation condition is given in (8). R_s is the source resistance, which is typically 50Ω. As size and current of the transistor M4 is made small due to the gm-boosting effect, the resistance R_o can be quite large as compared to R_s, which further multiplied by the factor of 2 increases the gain by 6-dB.

$$G \cong 2 * \frac{|A_{+}|R_0}{|A_{+}|R_s} = 2 * \frac{R_0}{R_s} \quad (8)$$

The lower end of the bandwidth is limited by the coupling capacitor C1, source resistance (R_s) and the input resistance (R_{in}) of the amplifier as shown in (9).

$$f_l = \frac{1}{2\pi(R_{in} + R_s)C_1} = \frac{1}{4\pi(R_{in})C_1} \quad (R_s = R_{in}) \quad (9)$$

However, higher cut-off frequency is mainly dominated by C_{gs} of the M0 and M1 transistor. Due to the cascode configuration by the transistor M2, the miller effect is very minimum. By including the miller capacitance, the mathematical expression for higher cutoff frequency is given in (10).

$$f_h = \frac{1}{\pi R * \left(\left(1 + \frac{g_{m0} + g_{m1}}{g_{ds0} + g_{ds1}}\right) * (C_{gd0} + C_{gd1}) + (C_{gs0} + C_{gds1})\right)} \quad (10)$$

IV. Implementation And Results

To divert output from the amplifier either to the receiver or to the antenna through 50Ω driver, a switch is required, which is implemented using transistors. Similarly, for off-chip testing of the low noise amplification on the VNA/Spectrum analyzer, 50Ω buffer is required, which is implemented using

a simple source follower. To deliver power from the voltage amplified signal from the amplifier to a 50Ω antenna, a driver circuit is used. This driver circuit is also a source follower amplifier. This source follower amplifier will drive 50Ω antenna with high power.

Skywater 130nm CMOS is an open-source process design kit (PDK) released by Skywater foundry and Google [14]. The aim is to make an open-source community of VLSI design with the process design kit that is compatible with open-source EDA tools. Skywater 130nm technology has the following salient features [15]:

The technology stack is shown in Fig. 12. The first metal layer is local interconnect, used for local connections of standard cells. Metal 2,3,4 are used for local and global routing. Metal 5 is the thickest metal layer and hence can be used to make high-quality passive structures like on-chip inductors, transformers, transmission lines, etc. The two mimcaps are implemented with CAPM and CAP2M layers. VIA1-VIA4 are via connections from metal1 to metal5. Metal 1 to local interconnect layer connection is made with the via called mcon. The layout of the proposed bi-directional amplifier designed in skywater 130nm PDK is shown in Fig. 13. The active chip area of the design is 204x166μm^2.

Post layout simulation is performed to verify the functionality of the netlist extracted against the layout. The post layout S11 plot of bi-directional amplifier is given in Fig. 14. Similarly, the noise figure plot of the amplifier is given in Fig. 15. It is evident that the noise figure has somewhat improved, due to the lack of any extracted resistance at the input which typically increases the noise figure. Likewise, the gain comparison of the amplifier in the two states (LNA on & PA off, or PA on & LNA off) is shown in Fig. 16 and Fig. 17 respectively. Here, again, it is evident that the gain is higher than the schematic simulation due to lack of any series resistance extracted from interconnects. Likewise, the gain in PA mode is lower as compared to LNA due to the fact that an additional buffer is also present in the path when PA is ON and LNA is OFF.

V. Comparison With State-Of-The-Art

The comparison with state-of-the-art is given in TABLE I. The proposed design in this work has superior performance in terms of the area, gain and output power. The area reduction is achieved mainly because this work does not include any inductors. A single inductor employed at this frequency range can typically be larger than the rest of the core circuit. The proposed bi-directional scheme in this work can deliver almost 10 times more power than the state-of-the-art bi-directional amplifiers.

VI. Conclusion

A single circuit that can perform both functionalities of LNA and PA in an RF transceiver denoted as BDA will not only reduce power but also on-chip area. This would prove instrumental for applications where the supply is provided by batteries. Hence, this paper presented a sub-5 GHz BDA for TDD applications implemented on skywater CMOS 130nm process. The design achieves voltage gain of 25.55dB in LNA mode while 20.38dB in PA mode with bandwidth of 1-4.5GHz. The noise figure is less than 3.5dB with input matching of -10dB in the entire band with 58mW power.

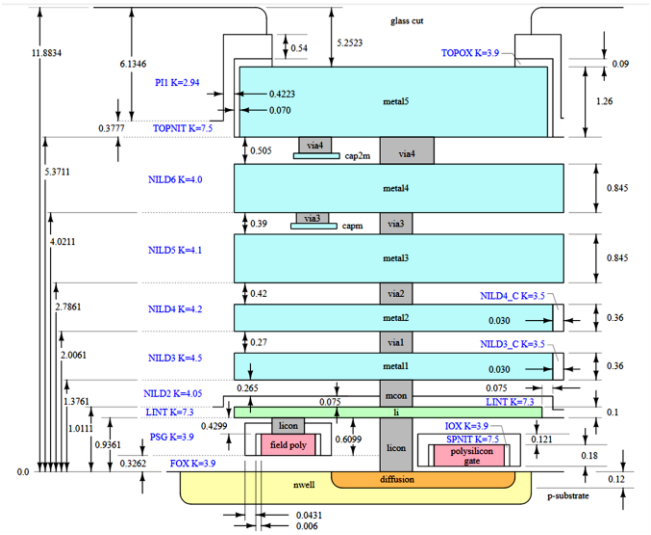


Fig. 12. Skywater 130nm CMOS Process Stack [15]

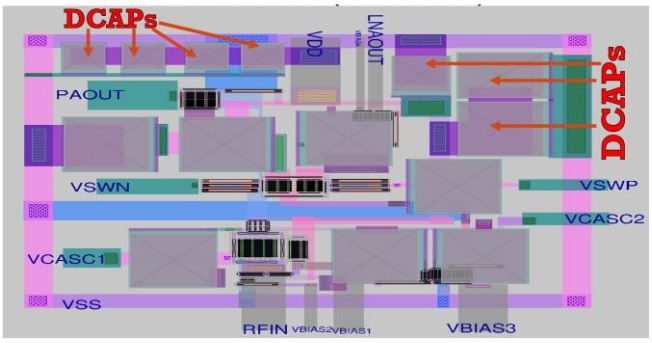


Fig. 13. Complete layout of the bi-directional amplifier in magic VLSI

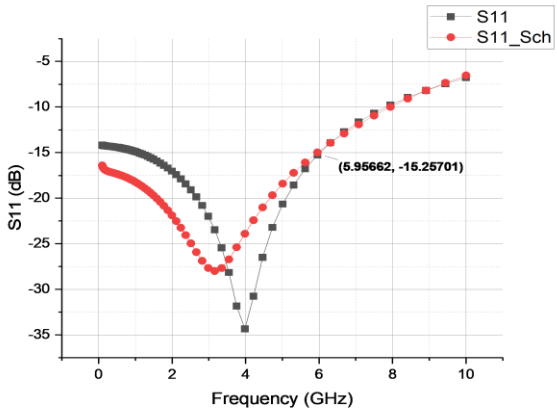


Fig. 14. S11 plot of the proposed bi-directional amplifier

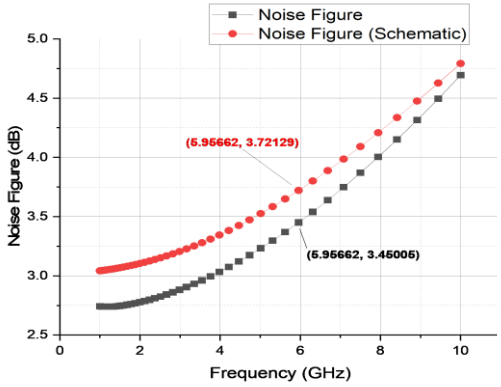


Fig. 15. Noise Figure plot of the Bi-directional amplifier

TABLE I. PERFORMANCE COMPARISON WITH STATE-OF-THE-ART

	This Work	[13]	[12]
Frequency (GHz)	1-4.5 GHz	3-20	5.5-14
Technology	130nm CMOS	130nm CMOS	130nm CMOS
Topology	CS-CG-NC 2-stage Inductor less	CS Distributed with multiple inductors	CS distributed with multiple inductors
Gain (dB)	25.55 (LNA) 20.38 (PA)	11	6.2
Area	0.034 mm^2	0.81 mm^2	0.23 mm^2
Noise Figure	<3.5 dB	3.2-6.5 dB	<6.1 dB
Input Matching	<-10 dB	<-10 dB	<-11 dB
DC power	58 mW	68 mW	43 mW

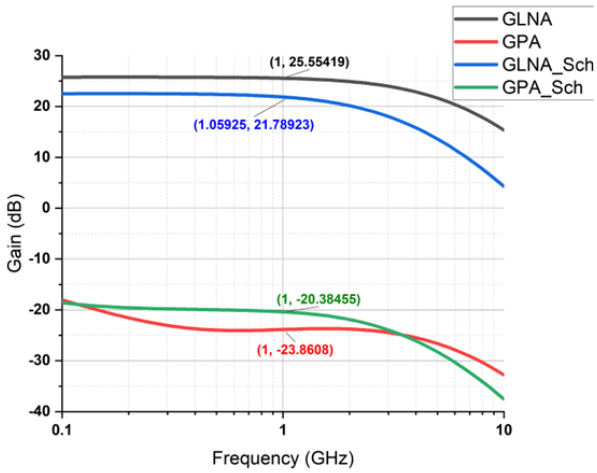


Fig. 16. Gain Comparisons of the post layout and schematic when LNA is on and PA is off

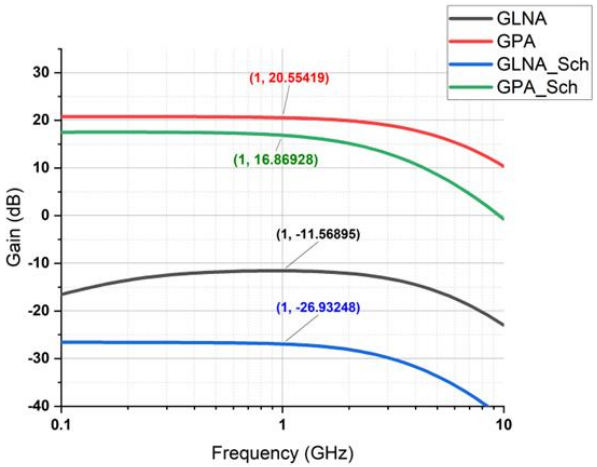


Fig. 17. Gain Comparisons of the post layout and schematic when LNA is off and PA is on

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