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Wideband Push-Pull Class E Amplifier for RF Power Delivery

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Wideband Push-Pull Class E Amplifier for RF Power Delivery

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***Abstract*—This paper presents the design and implementation of a 13.56 MHz push-pull Class E power amplifier with broadband capabilities. The Class E amplifier utilizes SiC MOSFETs with a custom current-source resonant gate driver. Because the amplifier is a push-pull structure, we design and implement a balun that converts the differential output into a ground-referenced output. This work experimentally demonstrates the proposed amplifier delivering over 1 kW power to a 50 Ω load impedance.**

***Index Terms*—Class E, Power Amplifiers, Balun, Resonant Gate Drive, Reactance Compensation**

I. Introduction

13.56 MHz power amplifiers (PAs) are essential constituents for radio frequency (RF) plasma-generating applications, including cleanroom etching chambers, CO_2 reforming, and satellite thrusters [1]–[3]. In many of these systems, the PAs are also required to deliver constant RF power within a bandwidth, typically between $\pm 5\%$ of the center frequency. The purpose of this broadband capability is to allow frequency tuning to adjust the impedance of the plasma [1]. Fig. 1 shows a simplified block diagram of a plasma system often employed for wafer etching in semiconductor processing. While the plasma load impedance can be variable, the PA interfaces with an automated tunable matching network, which adjusts the load impedance seen at the PA's output to 50 Ω. This work focuses on the design of the PA stage, including the broadband topology, resonant gate drive, and the balun stage. We demonstrate a 1 kW push-pull Class E operating between 12.56 to 14.56 MHz when driving a 50 Ω load. To enable high-power operation, the PA employs 1.2 kV silicon carbide (SiC) power metal-oxide-semiconductor field-effect-transistors (MOSFETs), where we utilize a custom resonant gate drive to provide the gate waveforms for the SiC devices. This work discusses the PA circuit design in Section II, the resonant gate drive design for the SiC MOSFETs in Section III, and the balun design in Section IV. Section V highlights the experimental results of this work, and Section VI concludes this paper.

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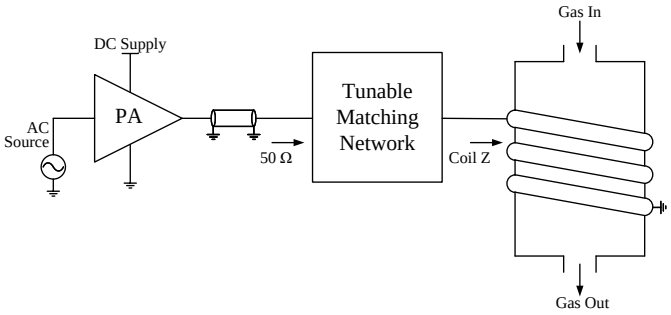

Fig. 1: Block diagram of a conventional plasma system.

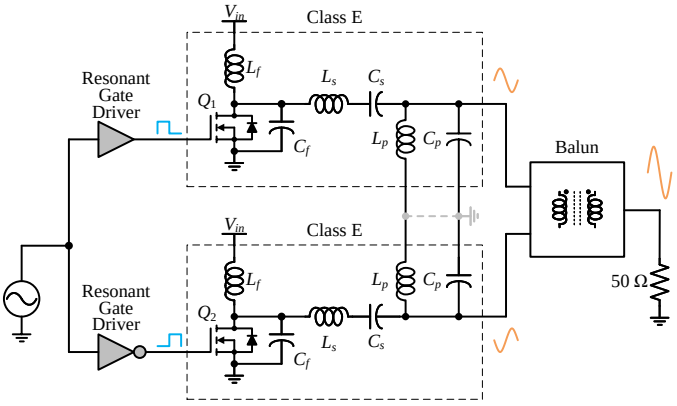

Fig. 2: Schematic of the wideband push-pull Class E PA. The midpoint between the two L_p and C_p components acts as a virtual ground.

II. Power Amplifier Design

For the topology, we use a push-pull Class E circuit shown in Fig. 2. The circuit employs two individual Class E stages driven with a 180° phase shift. The push-pull implementation allows the output voltages of the Class E circuits to be differentially summed, eliminating even harmonics in the total output voltage. A push-pull scheme provides the advantages of easier output filtering through even harmonic elimination, input current ripple cancellation, and increased output power capability. However, the major drawback is that a balun must be incorporated if the load is ground-referenced.

The Class E topology is one of the earliest published dc-ac resonant topologies using only a single ground-referenced switch [4]. The topology is a common and favorable circuit choice for MHz switch-mode PAs as the switching device has a ground-referenced source and achieves zero voltage switching (ZVS) and zero voltage derivative switching (ZVDS), eliminating frequency-dependent switching loss and minimizing the circulating current throughout the circuit [5]. For this work, we utilize the parallel circuit Class E variant, where the input inductor L_f forms a parallel resonance with the device's parallel capacitance C_f rather than acting as a pure choke inductor [6].

The Class E circuit can also operate across a wide bandwidth by incorporating a reactance compensation network [7], [8]. Reactance compensation is a method to tune a resonant network to maintain a relatively constant or controlled impedance phase angle across a bandwidth. Reference [9] is one of the earliest papers to demonstrate a broadband Class E amplifier using reactance compensation, where the series output network has a fixed quality factor to control the reactance shift across frequency, To allow more degrees of freedom, [10] and [11] incorporate a series (L_s and C_s) and a parallel LC (L_p and C_p) output network as shown in Fig. 2, where the output network can also be used for harmonic filtering. Equation (1) lists the component design equations for the wideband parallel circuit Class E, where Q_s and Q_p are the quality factors of the series and parallel output resonant networks respectively.

$$R_L = \frac{1.365V_{in}^2}{P_o} \tag{1a}$$

$$L_f = \frac{0.732R_L}{\omega} \tag{1b}$$

$$C_f = \frac{0.685}{\omega R_L} \tag{1c}$$

$$L_s = \frac{Q_s R_L}{\omega} \tag{1d}$$

$$C_s = \frac{1}{\omega Q_s R_L} \tag{1e}$$

$$L_p = \frac{R_L}{\omega Q_p} \tag{1f}$$

$$C_p = \frac{\omega R_L}{Q_p} \tag{1g}$$

To properly design the reactance compensation network, [11] calculates that Q_s and Q_p has the relationship in (2).

$$C_f + \frac{1}{\omega^2 L_f} = \frac{2}{\omega R_L}(Q_s - Q_p) \tag{2}$$

Thus, the single degree of freedom for the circuit design is Q_s, which also regulates the harmonics of the Class E circuit's output voltage. If Q_s is increased, the harmonic content at the output is reduced, but the bandwidth of the PA shrinks.

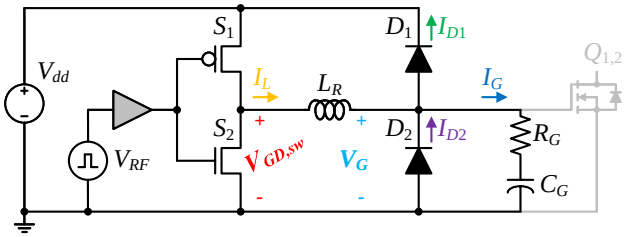

Fig. 3: Schematic of a resonant current source gate driver studied in [13].

III. Resonant Gate Drive

A. Gate Drive Operation

SiC power devices are challenging to utilize at MHz frequencies due to the gate drive requirements. The turn-ON voltage for commercial SiC devices is typically between 15 to 20 V, whereas GaN devices are around 5 V [12]. The higher enhancement voltages increase the gate driver loss based on (3), where $P_{G,conv}$ is the power loss of a conventional gate driver, f is the switching frequency, C_G is the gate capacitance, and V_{dd} is the turn-ON voltage.

$$P_{G,conv} = fC_G V_{dd}^2 \tag{3}$$

The gate capacitance C_G in SiC MOSFETs is also four to five times greater than in GaN high-electron-mobility transistors (HEMTs). Therefore, developing a custom gate-driving solution with high turn-ON voltages, fast transients, and low power dissipation is imperative for SiC MOSFETs switching at MHz frequencies.

For this work, we implement the gate-driving topology as a resonant current source gate driver developed in [13]. The schematic for the topology is shown in Fig. 3. Based on the waveform diagram in Fig. 4, the gate driver's operation can be described by three consecutive stages in a periodic cycle.

- **Stage 1:** Inductor current I_L flows from ground to V_{dd} through D_2 and S_1 (anti-parallel diode). V_G is clamped to ground until I_L reaches 0.
- **Stage 2:** D_2 turns OFF and an under-damped RLC circuit charges C_G. As I_L flows to C_G, V_G rises to V_{dd} and I_L reaches its peak value before D_1 turns on.
- **Stage 3:** D_1 turns on and I_L freewheels through D_1 and S_1. V_G is clamped to V_{dd}. Because the inductor current I_L lags behind the switching node voltage $V_{GD,sw}$, the half-bridge switches S_1 and S_2 can achieve ZVS, enabling low gate driver loss at MHz frequencies.

The gate drive topology in [13] is schematically identically to the gate driver proposed by Chen *et al.* in [14]. However, the totem pole half-bridge in the current source gate driver proposed by Chen *et al.* does not achieve ZVS and requires the duty cycle of S_1 and S_2 to be equivalent to the short transition times of the gate voltage, making it unsuitable for MHz operation.

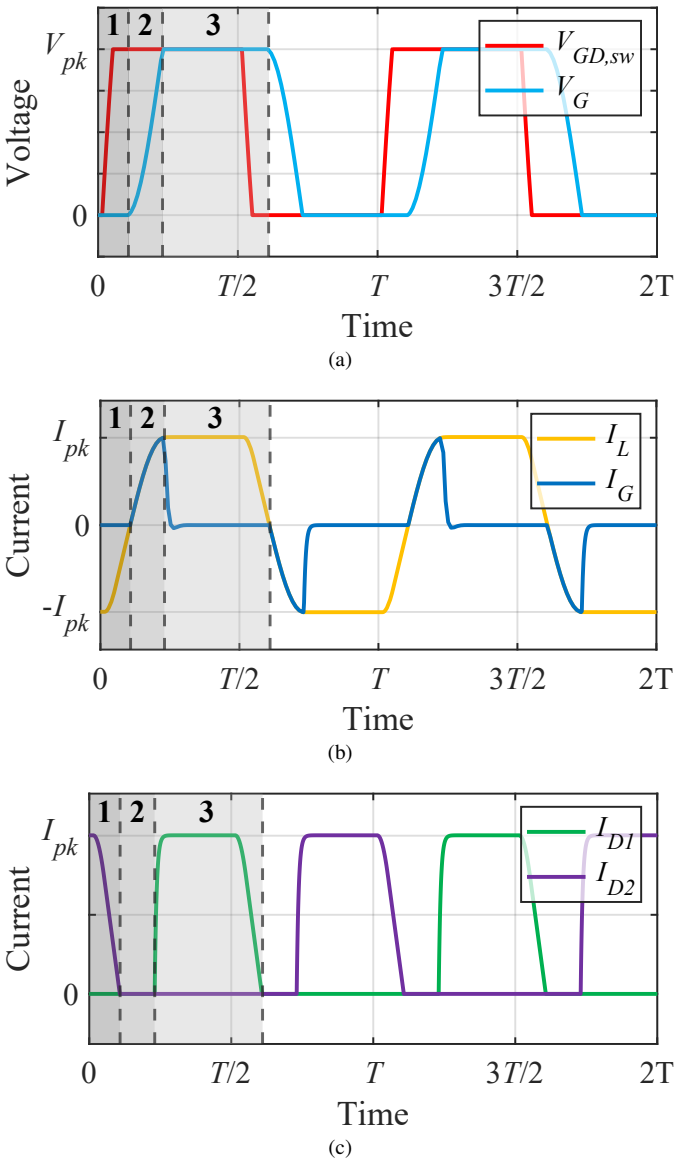

Fig. 4: (a) Example voltage waveforms of the resonant gate driver for two switching cycles. The three different stages of the gate drive operation are shaded in gray. (b) Example waveforms of the inductor current and gate current. (c) Example waveforms of the diode currents.

B. Power Dissipation

The resonant gate driver's power loss depends on the inductor's current amplitude I_L and the parasitic resistances distributed throughout the network. Typically, the diode conduction loss and the gate resistance conduction loss dominate the total loss due to the forward voltage of diodes D_1 and D_2 (~ 0.4 V) and the large intrinsic gate resistance of the SiC MOSFET, typically on the order of a few Ω's. The inductor's current amplitude depends on the desired transition time t_r of the gate voltage. A faster transition requires a greater current peak and a smaller L_R, which increases the driver's loss. From [13], the gate driver's loss is expressed through Equation (4),

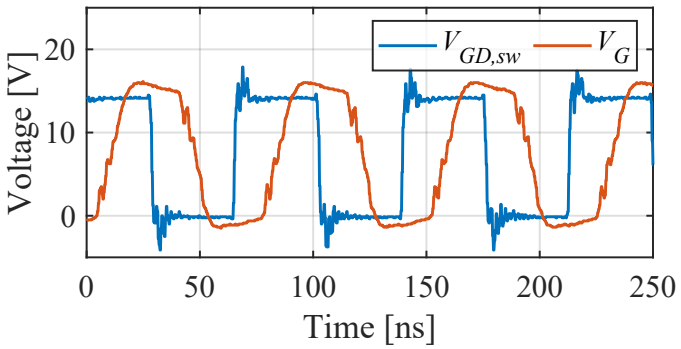

Fig. 5: Ratio of gate power loss from the resonant driver versus the conventional driver across frequency for a device with a 330 pF gate capacitance, 2.5 Ω gate resistance, and 15 V turn-ON voltage.

where k is the transition period of the gate waveform ($k = \frac{t_r}{T}$) and V_D is the forward voltage of diodes D_1 and D_2.

$$L_R = \left(\frac{2}{\pi}\right)^2 \frac{t_r^2}{C_G} \tag{4a}$$

$$I_{pk} = (V_{dd} + V_D)\sqrt{\frac{C_G}{L_r}}\left(1 - \frac{\pi}{2}R_G\sqrt{\frac{C_G}{L_R}}\right) \tag{4b}$$

$$P_{G,res} = \frac{2}{3}kR_G I_{pk}^2 + (1-2k)I_{pk}V_D \tag{4c}$$

Typically, k is around 0.1. Fig. 5 plots the calculated ratio of the resonant gate driver's power loss versus the conventional gate driver's power loss ($P_{G,res}/P_{G,conv}$) for an example device with 2.5 Ω gate resistance and 330 pF gate capacitance. It is evident from this figure that the resonant gate driver can conserve roughly 50% or more gating power at an appropriate frequency.

IV. Balun Design

In applications where the load is ground-referenced, push-pull amplifiers require a balun stage such that the differential output can drive a single-ended load. A common balun structure is a center-tapped transformer where the differential voltages and currents can be combined at the input and proportionally transferred to the output. An alternative structure is shown in Fig. 6, which is a center-tapped transformer separated as two individual transformers, with the primary windings connected in series and the secondary windings in parallel. The advantage of this approach is that utilizing two separate transformers allows more winding window space. To properly design the balun, the two transformers must be identical. Implementing identical transformers is challenging at high frequencies since the windings and the coupling coefficient must be identical. This work overcomes this challenge by presenting a balun design that can be implemented with non-identical transformers.

To start, in the transformer's cantilever model, the effective turns ratio (n_1 and n_2) and the leakage inductances (L_{l1} and L_{l2}) must be the same to achieve an effective balun.

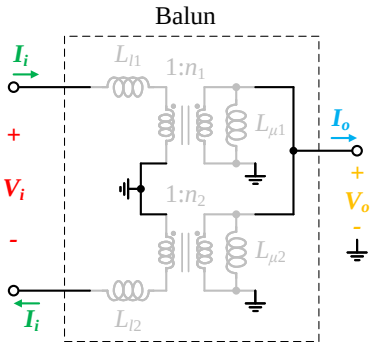

Fig. 6: Balun using two identical transformers in series at the input and parallel at the output. The transformers (in gray) are in cantilever form.

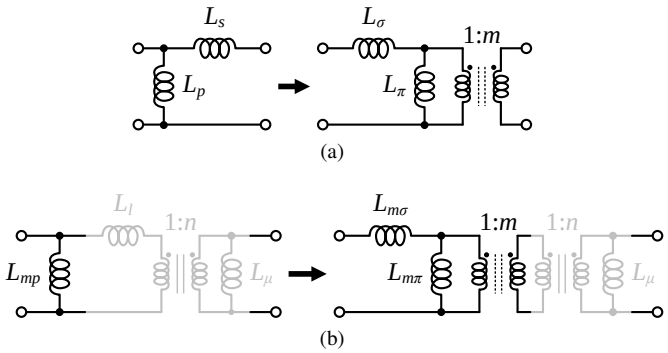

Fig. 7: (a) Shunt-series inductor network reversal creating a voltage gain of m at the output. (b) Incorporating the network reversal with a transformer to fine-tune the effective turns ratio (mn) of the transformer.

The magnetizing inductances ($L_{\mu1}$ and $L_{\mu2}$) are in parallel at the output so they do not need to be identical. The leakage inductances of the transformers can be easily matched by adding series inductors at the inputs. However, the effective turns ratio is more difficult to control since ideal transformers do not exist. A method of creating an effective turns ratio using pre-existing lumped elements is through a tapped inductor matching network as shown in Fig. 7a [15], [16]. By reversing the shunt-series network of L_p and L_s into the series-shunt network of L_σ and L_π, an effective turns ratio of m is created at the output, where (5) calculates the parameter values.

$$m = 1 + \frac{L_s}{L_p}, \quad L_\sigma = \frac{L_s}{m}, \quad L_\pi = \frac{L_p}{m} \tag{5}$$

To finetune the effective turns ratio of any transformer, we can insert a shunt inductor L_{mp} at the input as shown in Fig. 7b. L_{mp} and the transformer's leakage inductance L_l creates a shunt-series tapped inductor network. In Fig. 7b, the effective turns ratio becomes mn, where m is adjusted by L_{mp} and n is the transformer's innate turns ratio.

Thus, a balun with two non-identical transformers can be made by inserting shunt inductors L_{mp1} and L_{mp2} as shown in Fig. 8a. L_{mp1} and L_{mp2} are tuned to equalize the effective turns ratio m_1n_1 and m_2n_2. Additionally, external series inductors L_{ms1} and L_{ms2} are added to match the series leakage inductances of the two transformers. Furthermore, m_1n_1 and m_2n_2 can be selected to provide a voltage gain N to provide impedance transformation. Equation (6) provides the design equations for L_{mp1}, L_{mp2}, L_{ms1}, L_{ms2}, m_1, and m_2 for two given transformers with parameters n_1, n_2, L_{l1}, and L_{l2}.

$$m_1n_1 = m_2n_2 = N \tag{6a}$$

$$L_{ms1} + \frac{n_1}{N}L_{l1} = L_{ms2} + \frac{n_2}{N}L_{l2} \tag{6b}$$

$$L_{mp1} = \frac{L_{l1}}{\frac{N}{n_1} - 1} \tag{6c}$$

$$L_{mp2} = \frac{L_{l2}}{\frac{N}{n_2} - 1} \tag{6d}$$

If an impedance transformation is undesired from the balun, particularly, the overall effective turns ratio N is desired to be 1, the top transformer can be eliminated since it provides no electrical functionality. Thus, for the top branch, only a series inductor L_{ms}, as shown in Fig. 8b, is required to match the effective leakage inductance of the bottom branch. L_{mp} must be finetuned so that the effective turns ratio is exactly unity. Equation (7) provides the design equations for the balun structure with unity voltage gain.

$$mn = 1 \tag{7a}$$

$$L_{ms} = \frac{L_l}{m} = nL_l \tag{7b}$$

$$L_{mp} = \frac{nL_l}{1-n} \tag{7c}$$

Note that for both balun designs, m must be greater than 1, which means that in Equation (7), n must be smaller than 1. Therefore, to properly design a unity gain balun, the primary winding must have more turns and/or greater self inductance than the secondary winding. For this work, we utilize the balun structure in Fig. 8b, as it requires a minimal component count of only two inductors and one transformer.

V. Experimental Results

A. Resonant Gate Drive

To demonstrate the previously discussed PA design, we construct a 1 kW push-pull Class E prototype centered at 13.56 MHz. The main power devices are 1.2 kV-rated G3R350MT12J SiC MOSFETs manufactured by GeneSiC. According to the datasheet, the gate requires 15 V to fully enhance the device [17]. Because very few commercial gate drive integrated circuits (ICs) suitable for MHz frequencies can operate on a 15 V supply, we utilize gallium nitride (GaN) transistors for the totem-pole switches (S_1 and S_2) and drive them using a commercial half-bridge gate drive IC. The diodes (D_1 and D_2) are MMBD301LT3G radio frequency (RF) Schottky diodes with low junction capacitance (under 2.4 pF). We connect four of the diodes in parallel for each

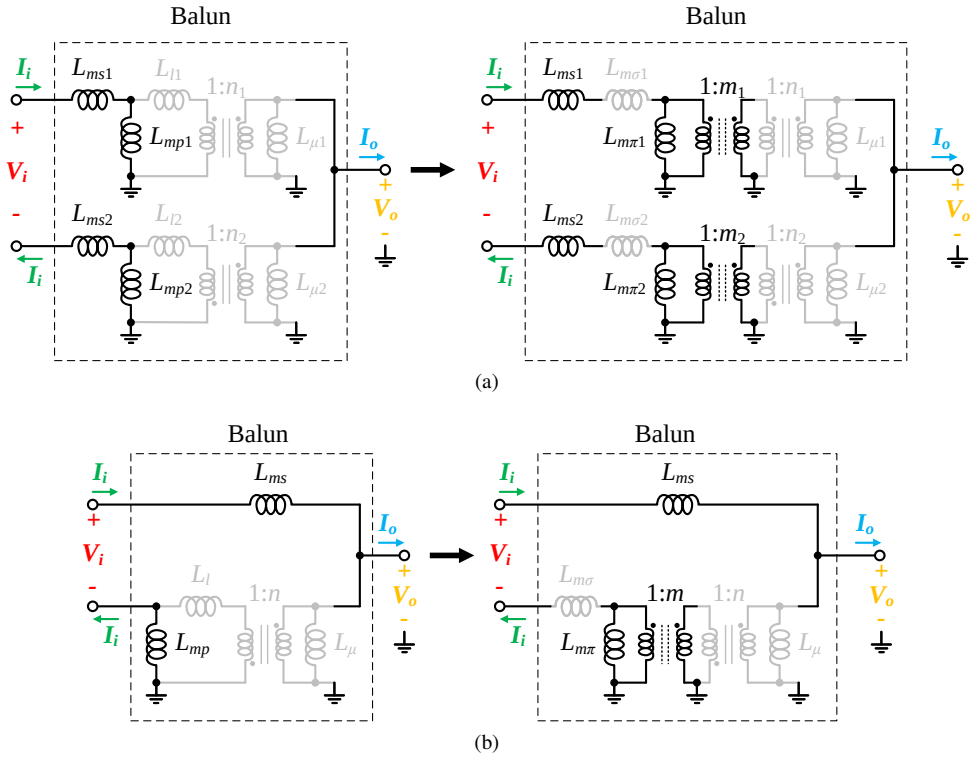

Fig. 8: (a) Final balun structure using two non-identical transformers with the effective turns ratio ($m_1 n_1$ and $m_2 n_2$) equalized using L_{mp1} and L_{mp2} and leakage inductances matched using L_{ms1} and L_{ms2}. The left schematic is the actual circuit while the right schematic shows the equivalent tapped inductor transform. (b) Alternative final balun structure with no impedance gain with fewer components and utilizing only one transformer.

TABLE I: List of components used in the resonant gate driver.

Component	Part Number & Value
S_1 & S_2	EPC8004, 40 V-rated eGaN power transistor from EPC
Half-Bridge Driver	LMG1210, 200-V half-bridge gate driver from Texas Instruments
D_1 & D_2	MMBD301LT3G, 30 V-rated Schottky diodes from onsemi ($\times 4$)
L_R	67 nH, 2 turns with 9567130302 core from Fair-rite
$Q_{1,2}$	G3R350MT12J, 1.2 kV-rated SiC MOSFET from GeneSiC, with $R_G = 2.5\ \Omega$ & $C_G = 331$ pF

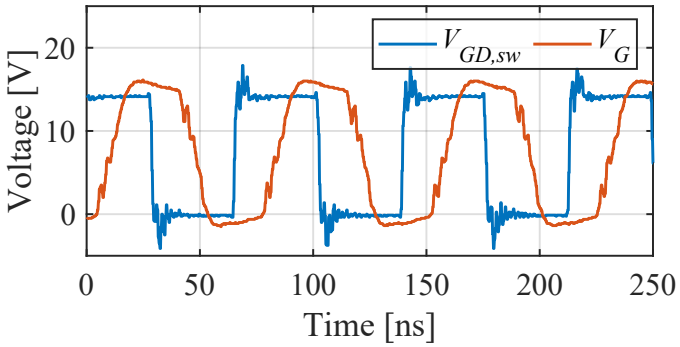

Fig. 9: Measured waveforms of $V_{GD,sw}$ and V_G of the resonant gate driver at 13.56 MHz.

in order to increase the current capabilities. To achieve a k value of 0.1, L_R must be approximately 67 nH according to (4a). L_R is a 2-turn inductor using planar cores of material 67 from Fair-rite, which can be easily gapped to finetune the inductance. Table I lists the components used in the resonant gate driver.

Fig. 9 also shows the resonant gate drive waveforms, where the gate driver is supplied from a 15 V rail with control signals from an Agilent 81150A signal generator. It is evident from the waveform of $V_{GD,sw}$ that switches S_1 and S_2 achieve ZVS due to the turn-ON of the intrinsic body diodes. To compare the performance of the resonant gate driver with a conventional gate driver, we simply removed the L_R such that S_1 and S_2 serve as a totem pole. The gate power loss is 1.35 W per FET using the resonant driver, while the conventional gate driver dissipates 1.8 W. Thus, the resonant gate drive improves the power dissipation by 25% and conserves a total of 0.9 W for the power amplifier.

B. Power Amplifier Measurements

The prototype operates on a 200 V dc supply voltage such that the maximum drain-to-source voltage across the SiC MOSFETs would be roughly 800 V. The PA delivers the RF power to a 50 Ω RF dummy load, meaning each Class E

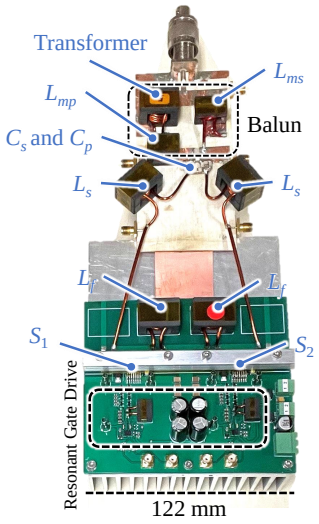

Fig. 10: Photograph of the push-pull Class E prototype.

TABLE II: List of components used in the power amplifier prototype.

Component	Part Number & Value
L_f	940 nH, 4 turns with 9567250802 core from Fair-rite
C_f	73 pF, absorbed by the C_{oss} of the G3R350MT12J SiC MOSFET
L_s	2377 nH, 5 turns with 9567250802 core from Fair-rite
C_s	60 pF, C0G dielectric ceramic capacitors rated for 1 kV
L_p	1107 nH, absorbed by the balun's L_μ in parallel with $L_{m\pi}$
C_p	124 pF, C0G dielectric ceramic capacitors rated for 1 kV
L_{ms}	234 nH, 2 turns with 9367054002 core from Fair-rite
L_{mp}	1700 nH, 7 turns with 9567200602 core from Fair-rite
Transformer	5 turns primary, 4 turns secondary with 9567250802 core from Fair-rite

stage drives a 100 Ω load impedance and delivers 500 W. Fig. 10 shows an image of the prototype. The component values of the amplifier are calculated using Equation (1), and Table II lists the values of the inductors and capacitors in the amplifier. For the reactance compensation network, we chose Q_s to be 2 and Q_p to be 1.06 such that the magnetizing inductance of the balun can be fully integrated into L_p and the leakage inductance can be integrated into L_s. The balun stage with unity voltage gain contains a transformer with 5 turns for the primary winding and 4 turns for the secondary winding. The effective turns ratio of the transformer n is 0.86, measured using a 2-port vector network analyzer (VNA), and the leakage inductance of the transformer is 272 nH. Based on Equation (7), m is 1.16, L_{mp} is calculated as 1700 nH, and L_{ms} is 234 nH.

Fig. 11 shows the time-domain waveforms of the drain voltage from 12.56 to 14.56 MHz. It is evident from Fig. 11 that ZVS and ZVDS are achieved across the 2 MHz bandwidth, indicating the proper design of the reactance compensation network. Additionally, the drain voltages of the SiC MOSFETs are symmetrical, meaning that the balun provides equivalent load impedances with a 180° phase shift to the stages of

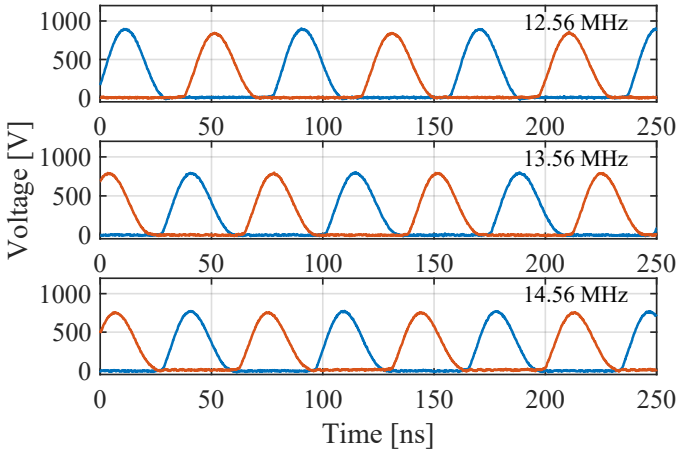

Fig. 11: Measured drain voltage waveforms across the switching devices of the 1 kW push-pull Class E prototype at 12.56, 13.56, and 14.56 MHz.

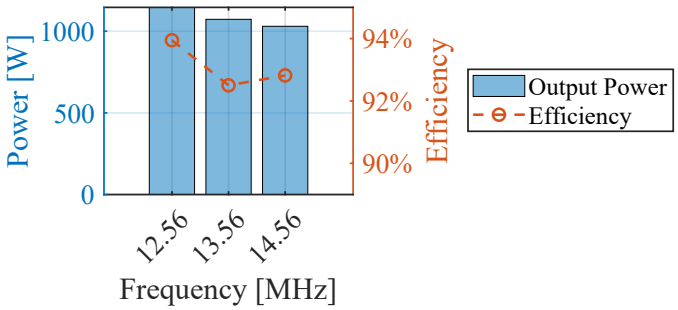

Fig. 12: Measured output power and drain efficiency (ratio of RF output power to the input power from the 200 V dc supply) of the prototype at 12.56, 13.56, and 14.56 MHz.

the push-pull converter. Lastly, Fig. 12 shows the power and efficiency measurements of the prototype.

VI. Conclusion

This work presents the design and implementation of a high-power push-pull Class E topology suitable for plasma generation applications. We utilize SiC switching devices to enable high-performance operation and incorporate resonant gate drivers to conserve gating power and enable fast transitions at MHz frequencies. We also present the design of a broadband balun with a reduced component count without using identical transformers, overcoming implementation challenges at high frequencies. As a result, we experimentally demonstrate a 1 kW push-pull Class E prototype.

Acknowledgments

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