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№ 5615

32 Bit Power, Area and Delay Efficient Carry Select Adder Using Modified 10T Full Adder

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May 26, 2021

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ABSTRACT

In VLSI design With the development in the technology, adder circuits and other all applications are concentrating on high speed and low power requirements. In many data processing CSLA is mainly used It is a faster adder. There is a scope for decreasing the power, area & increase in speed. In this paper, we proposed a system which is designed with CMOS modified 10T full adder. Here less number of transistors are utilized to design full adder. Cadence virtuoso tool is used in 90nm technology. This modified circuit works on pass transistor technology. 90nm technology with supply voltage 1.8V is used. It is designed using 2 inverters and pass transistors. We get full swing voltage at the output. So there is no degraded output for more number of inputs. In this newly designed full adder compare to existing 4T XNOR logic less number of transistors are used so area utilization and power is reduce.

Keywords: *Modified full adder, Carry Select adder, redundant circuit area, power and delay.*

1. Introduction

In all Electrical applications adders are mainly used. Millions of instructions are performed per second in microprocessors. In the elementary adder, each bit position sum is sequentially generated after sum has been done for previous bit and for next position carry propagated. Based on the arithmetic functions The computational circuits always designed. Many ways are used to design adders.

With implement and development in technology, VLSI design applications always concentrating in low power, area, delay and high speed. CSLA is designed by many authors. 3T and 4T XNOR full adders are designed to reduced the transistor counts. CLSA is said to be a fastest adder. In many data processing processors the CSLA is mainly used. The scope of CMOS technology is decreasing the power and area[1].

Author Ramkuumar and Harish M kittur used BEC converter instead of one more RCA circuit by this the power and area is reduced. Full adders are used for addition. The CSLA is designed using the Full adder. For different applications adders are designed differently. carry propagation delay is the main drawback of RCA. The simplest design is the RCA but main drawback is carry propagation delay[4].

Gate level modification is used significantly to reduce the area and power. The delay is slightly increased in this[4].

B. Sathyabhama, M. Deepika, and S. Deepthi designed the full adder using 8T full adder their main goal is to reduce the area and power. So they tried to reduce number of gates used. 8T transistor is used as basic building block for CSLA. They eliminated all redundant logic operations. For full adder design XNOR-XNOR circuits are the basic building blocks[2].

These circuits are mostly used in phase detector, Multipliers, parity checkers, DSP architectures, comparators, microprocessors etc[2].

XOR-XNOR full adder circuit is designed. Here 9T full adder is designed in 3T XOR style. New circuit is designed by the combination of transmission gate and pass transistors[3].

Here 3 transistors are used to design XNOR gate. They designed 8T full adder power and area is reduced[5]

1.1 Problem Statement

3T XNOR gate has drawback of non full swing voltage. Degraded output for more number of input bits. So in 2016 author Rashmi S.B and Veena Oli designed new design of 32 bit power efficient carry select adder using 4T XNOR gate. Here one more PMOS transistor is used to overcome these drawbacks but area is increased. To overcome this modified full adder is designed.

1.2 Our Contribution

The modified full adder is introduced it has very less number of transistors compare to existing design so the area, power is reduced, speed is increased. The CSLA designed by using modified full adder building blocks. The area, delay and power is completely reduced.

1.3 Organization of paper

The remaining of this paper is organized as follows: Section I provides the details of introduction. Section II provides methodology for existing and proposed modified design, its implementation and expressions used for the sum and carry. Section III provides CSLA designed using 10T full adder. Section IV provides simulated results. Section V provides tabular column of power delay.

2. Methodology

Existing methodology 3T XNOR Full Adder

To design the carry select adder authors proposed different logic styles. In existing full adder using 3T XNOR to minimize the transistors pass transistor logic has been adopted and gate number reduced to three. Normally we need 8 transistors to design XNOR gate. It is low power and area efficient but it has threshold voltage drop and

low output voltage swing. So to overcome this draw back one more PMOS is added by increasing the W/L ratio in the 4T XNOR design.

The operation of pass transistor logic is that it will pass the input signal to output. The circuit consists of two NMOS (M1 & M2) and one PMOS (M3). The M1 & M2 transistors source are shorted and connected to drain of PMOS (M3). The gate inputs of both M1 & M3 are shorted and connected to drain of M2 and input B. For drain of M1, gate of M2 and input A are connected. Source of PMOS (M3) is given to VDD. Output is taken at shorted node of PMOS's source and PMOS's drain. The 3T XNOR circuit is as given in below Fig 1.

The logic equation of XNOR is:

V out = A XNOR B

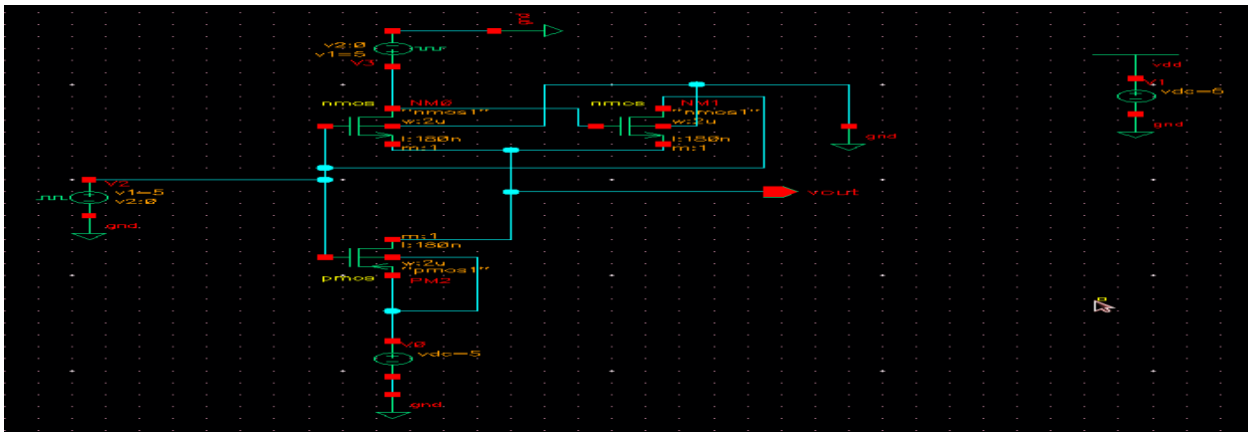


Fig.1 Full Adder using 3T XNOR gate

compact design of XNOR and MUX is as given in below fig.2 The FA circuit designed using two XNOR gate in order to generate sum and carry, multiplexer circuit is used. The MUX input are Cin and A inputs with control signal as XNOR output of first stage.

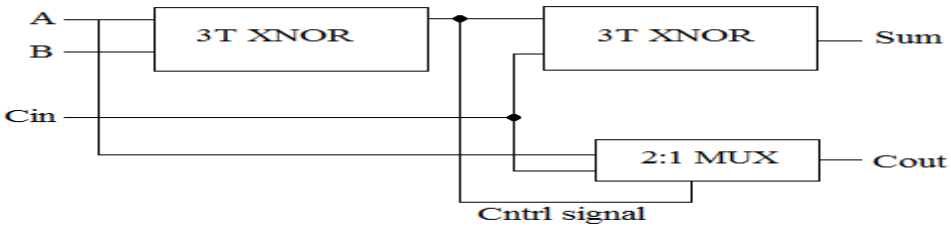


Fig 2. 3T XNOR Full Adder

The diagram illustrated above has compact design since it has compact structured

2.1 EXISTING METHODOLOGY 4T XNOR Full Adder

The previous circuit has non full swing voltage for inputs A (0, 1) and B (0, 0). The degradation occurs for inputs A =0 and B =1 due to nMOS-NM0 switching voltage and Vth also switch over to pMOS-PM1 before its turn OFF. To overcome this problem of early switchover of PM1 one pMOS-PM0 is used across the NM0 to behave as

transmission gate. For inputs A = 1 and B = 1 again there will be degraded output because of pMOS-PM1 due to its minimum V th. Due to this before it gives full voltage at the output PM0 will become OFF. To avoid this critical condition of sudden switchover the aspect ratio of PM0 is increased. Width of PM0 is kept constant and length is increased in step difference of 100nm from 250nm to 700nm to overcome degradation of output voltage. The below figure shows 4T XNOR Full Adder. Here to design full adder transistor count increased to 18 so utilized area is increased. But this design don't have degradation of 3T xnor circuit.

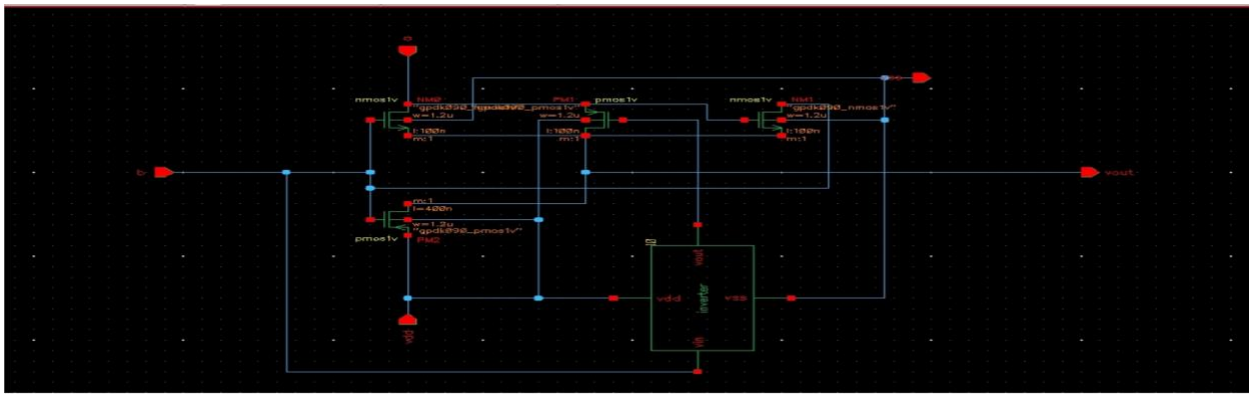


Fig 3. 4T XNOR Full Adder

The circuit operation can be given by expression as:
Sum out = ((A $\oplus$ B)' $\oplus$ C in)'

Cout = C (A $\oplus$ B)+ B (A $\odot$ B)

2.2 proposed methodology

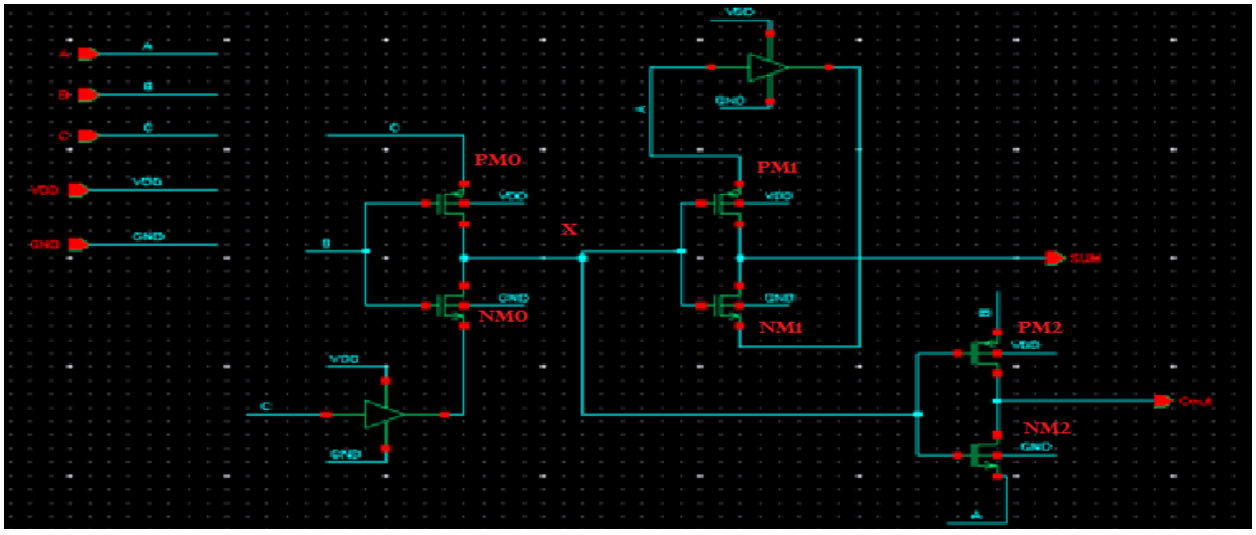


Fig.4 Modified 10T Full Adder.

The above Fig.4 is the modified full adder design. In this design less transistors are used compare to existing 4T XNOR full adder design and 3T xnor design. It works based on pass transistor logic. We get output x = b'c + b c'

(i.e b xor c). The pass transistors PM0 NM0 will pass the b' c & b c'. Output X= b'c + bc'. X output is the input for pass transistors PM1 and NM1. It will passes x'a + a'x. So at the output we get sum of full adder.

To get carry X is given as input for PM2 and NM2 pass transistors . We get carry output x'b +xa. We get carry output x'b +xa.

$$X = B'c + BC' = B \oplus C$$

$$SUM = X'A + X A'$$

$$= X \oplus A$$

$$= A \oplus B \oplus C$$

$$Carry = AC + BC + AB.$$

$$CARRY = X'B + XA$$

$$= (B \oplus C)'B + (B \oplus C)A$$

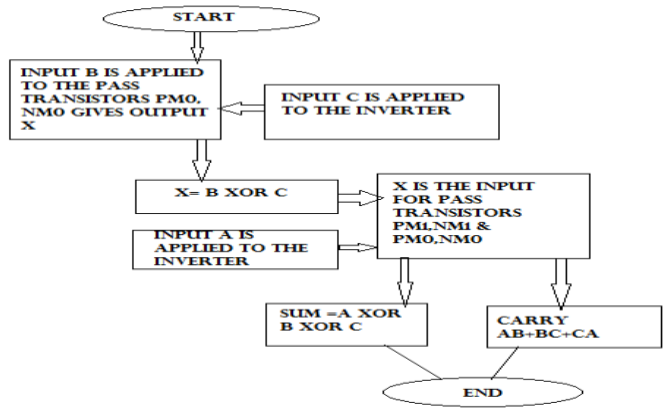
$$= (B'C' + BC)B + (B'C + BC')A$$

$$= BC + AB'C + ABC'$$

$$= C(B + AB') + ABC'$$

$$= AC + BC + AB$$

2.3 ALGORITHM



3. CSLA DESIGNED USING 10T FULL ADDER

The CSA is designed using 32 full adder blocks. RCA is designed for cin=0 and cin =1 and Multiplexer (2:1 MUX) is used. Here RCA1 is used for carry input Cin = 0. RCA2 is used for Cin1. MUX is used to select the final carry and um.

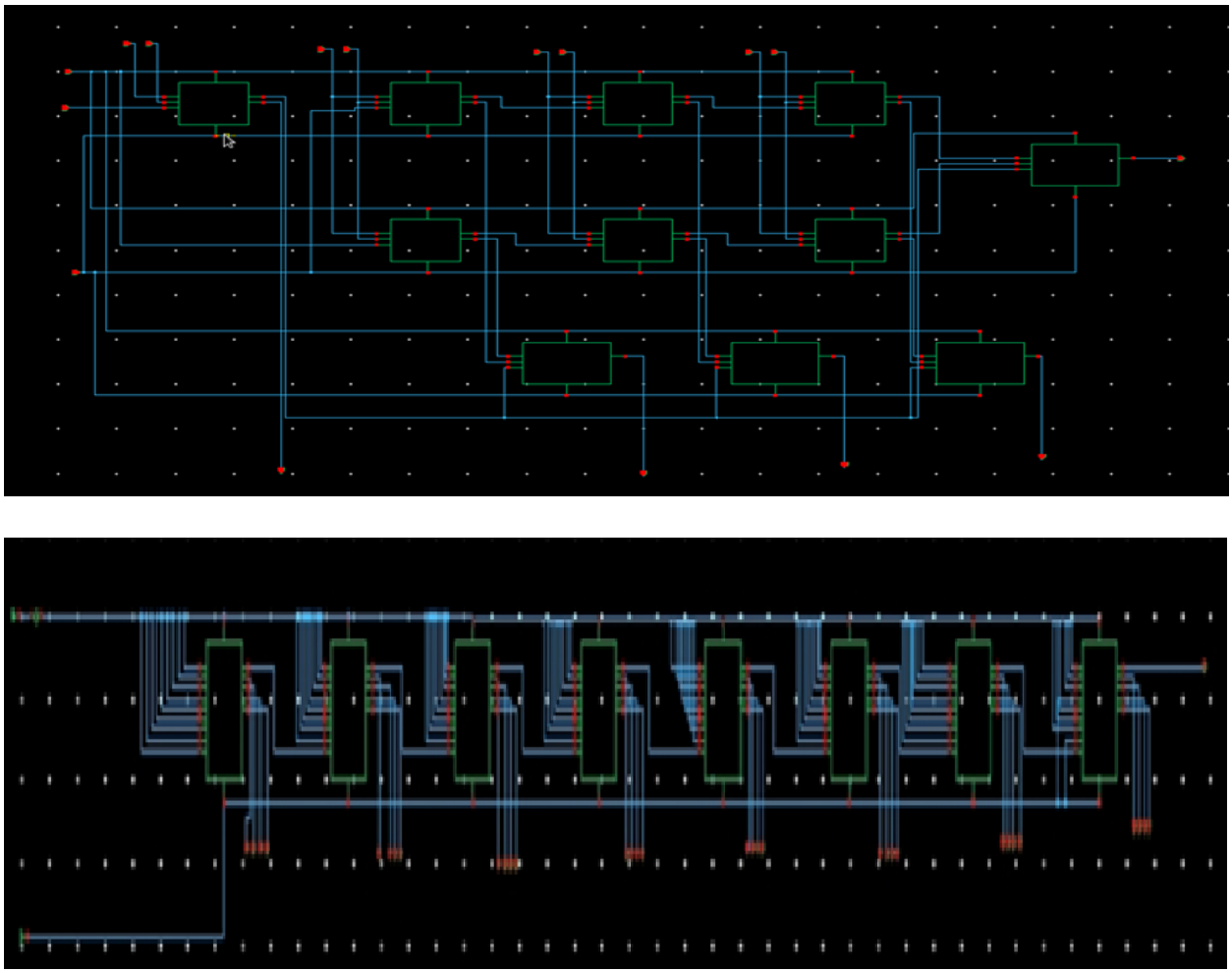


Fig.5 32bit CSLA design

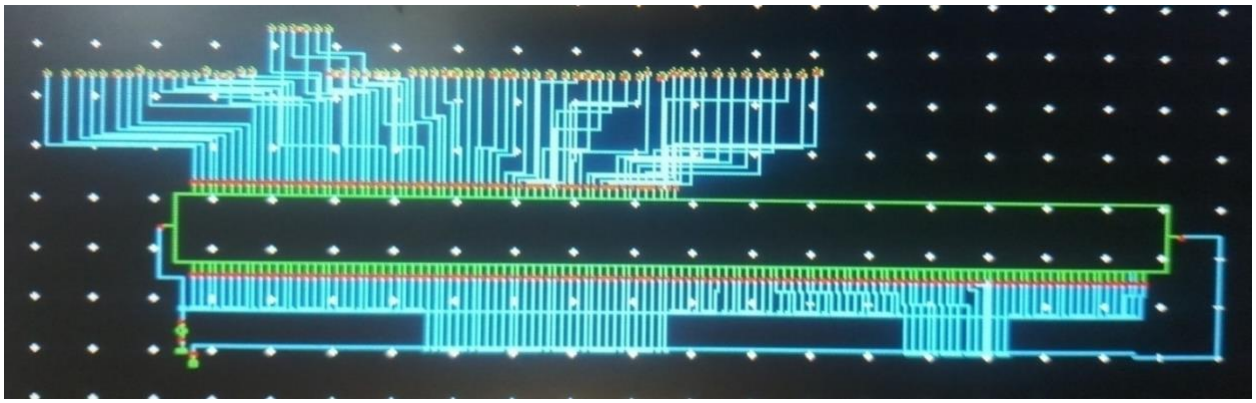


Fig. 6 CSLA test circuit

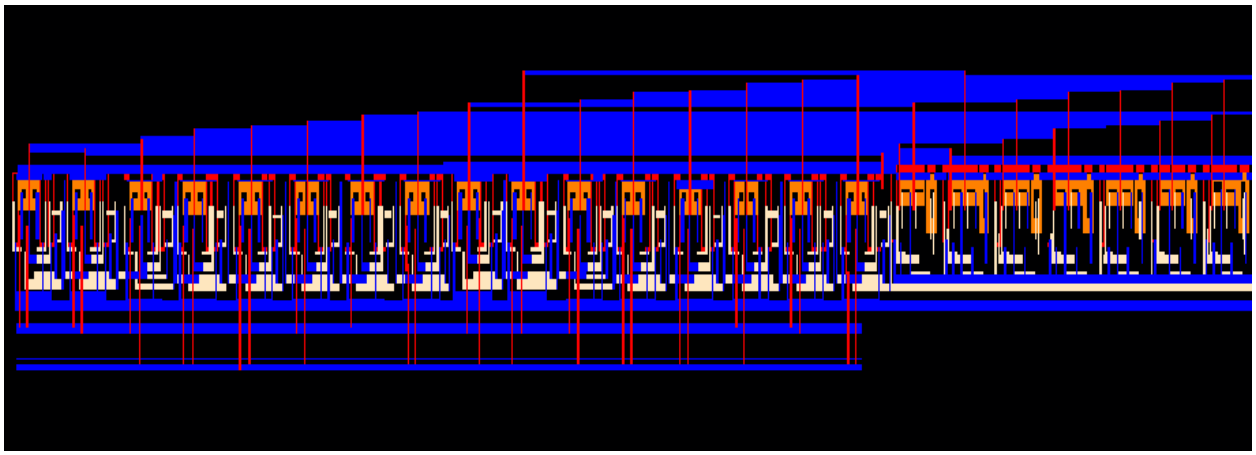


Fig.7 layout of CSLA

4. SIMULATION RESULTS

Cadence virtuoso 90nm technology is used for the simulation. This modified design is compared with the previous circuit of 4T XNOR and 3T XNOR gate. The power, area and delay is reduced Maximum. The power of the 4T XNOR gate Full adder circuit has more power but in the modified 10T full adder circuit power is reduced lot compare to that. It has full voltage swing at the output. Area and delay is also reduced. So the speed and accuracy of the design is increased.

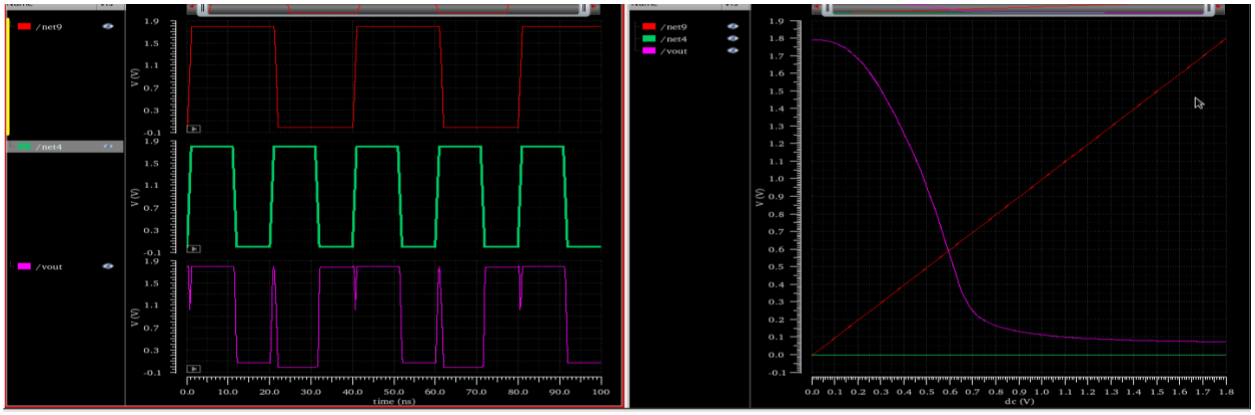


Fig. 8 4T XNOR output

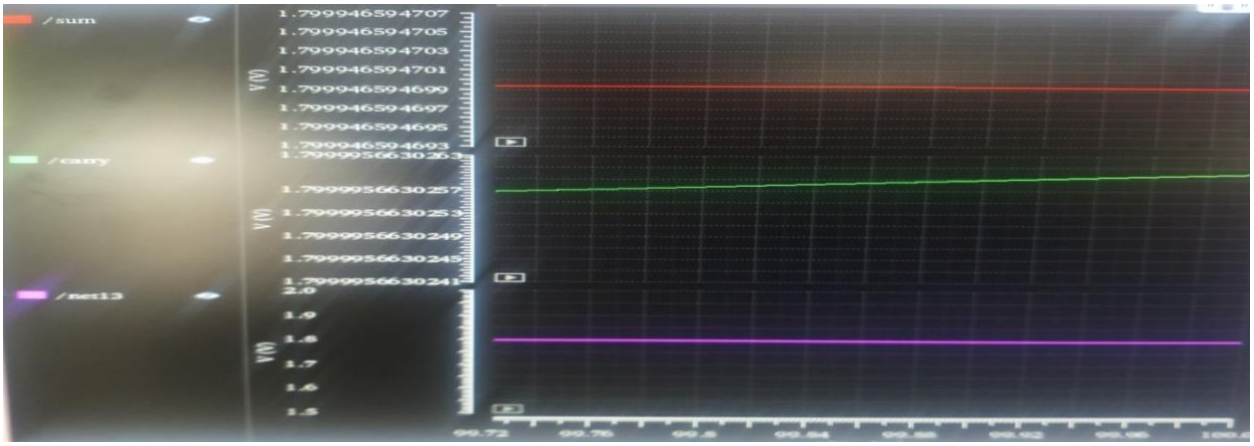
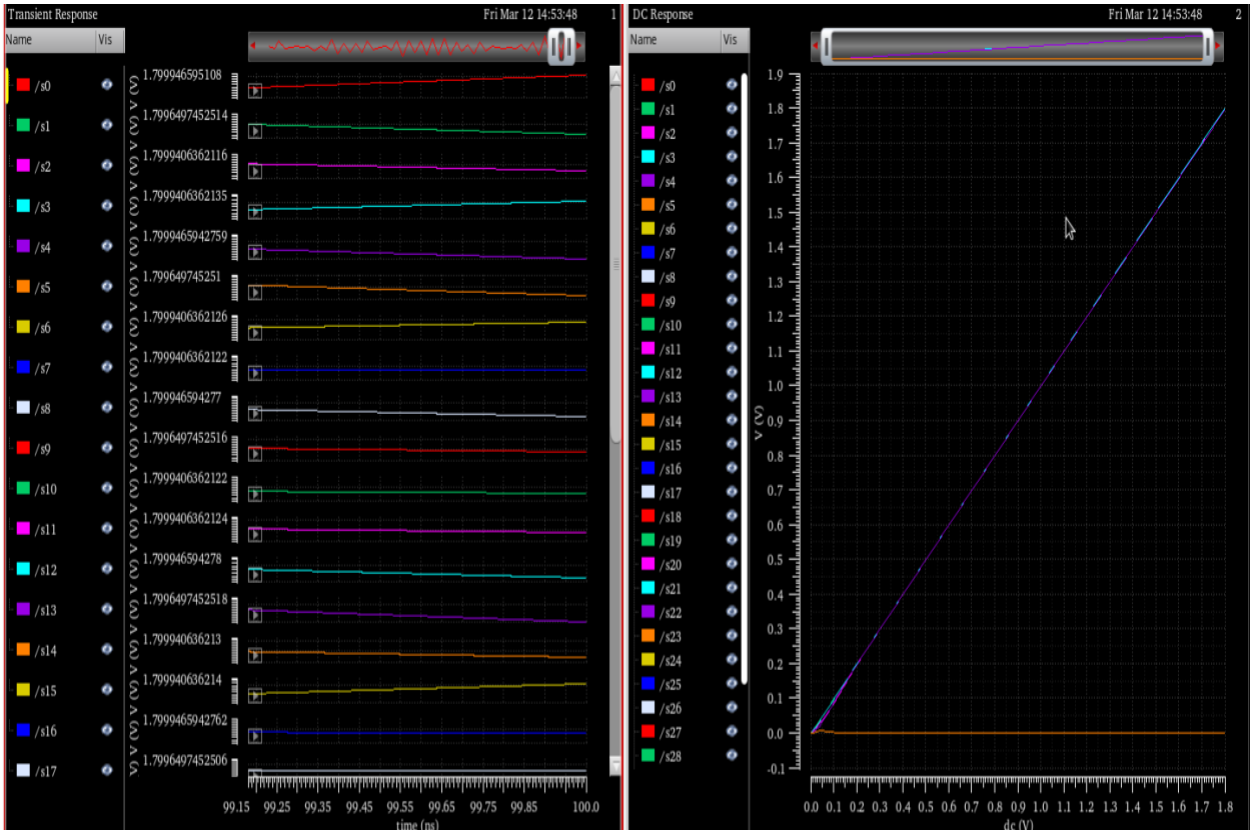


Fig. 8 modified full adder output

4.1 SIMULATED RESULT OF CSLA



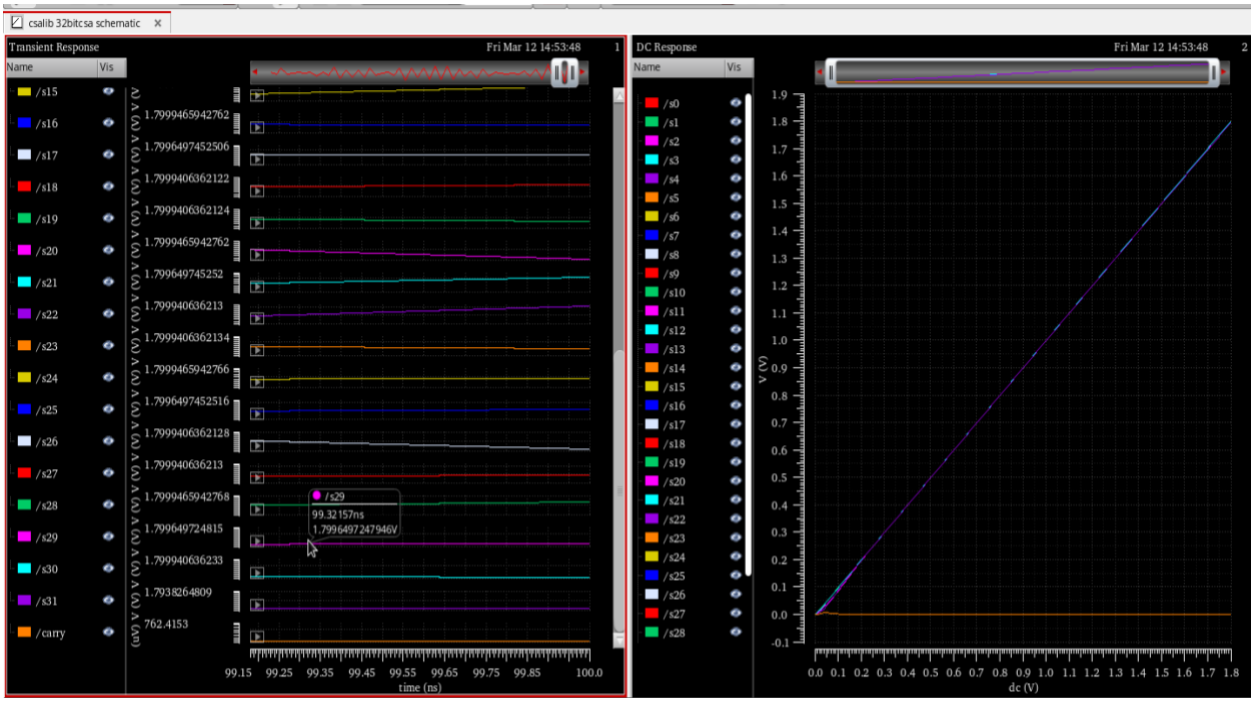


Fig. 9 CSLA OUTPUT

5. Tabular column

Various Circuits	Power utilization (mW)	Delay (ns)	Transistor count
4T XNOR FA	0.599	30.35	18
Modified 10T FA	0.33	20.86	10
Existing 8bit CSA	23.63	10.17	320
Proposed 8bit CSA	10.5	7.74	188
Existing 16 bit CSA	29.72	20.39	640
Proposed 16bit CSA	20.90	14.89	376
Existing 32 CSA bit	68.81	20.13	1300
Proposed 32bit CSA	43.69	15.16	752

The power, area and delay consumed by the existing circuits and modified circuits are compared. Also transistors utilized for various circuits are also compared. Results are tabulated as

6. CONCLUTION

32bit carry select adder using modified full adder and existing 4T XNOR carry select adder is analyzed in this proposed work for the parameters like area and power consumption. It is implemented for reduced power, area and delay with full voltage swing at the output. Here number of transistors used are very less 48% less compare to existing CSLA. There is no degraded output. 90nm technology is used so speed is also increased. Because of less transistors area is also reduced.

7. FUTURE SCOPE

The 8bit, 16bit 32bit CSLA is design modified and implemented. Compare to existing CSLA the modified CSLA power, area and delay is reduced. It has full swing output. Different optimization techniques can be applied for further reduce of area, power and delay. Further it can be extended for high bit word size.

8. ACKNOWLEDGEMENT

The author would like to thank Dr. Mahendra prashanth HOD & professor of *ECE department,* SJB institute of Technology, Bengaluru, India. for his support and motivation in completing this work.

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