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A Single-Trap Study of PBTI in SiON nMOS Transistors

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Abstract: To accurately study positive bias temperature instability (PBTI) in nanoscale SiON nMOS transistors we make use of the time-dependent defect spectroscopy (TDDS) and examine the device performance degradation at the single-defect level. Contrary to what is visible in large-area devices, our investigations clearly reveal charge trapping at both electron and hole traps contribute to the overall drift of the threshold voltage in these devices. Even though only electron trapping is typically considered for PBTI we observe that hole traps account for around 20% of the total threshold voltage drift. To evaluate the impact of single-defects on the device performance we characterize the charge trapping kinetics of a number of defects, which can be explained employing a two-state defect model. In our approach we consider charge trapping due to defect/channel and defect/polygate interactions for the defects. From the extracted trap levels and trap depths we conclude that hole traps reside in the middle of the insulator while electron traps are located closer to the SiON/Si interface. Finally, the extracted trap parameters are fully consistent with defect candidates from DFT calculations.

Introduction: A large number of single-defect studies have been performed considering NBTI in devices employing in SiON or SiO_2 as gate insulator[1–9] so far. However only little attention has been paid to PBTI in nMOS devices. Since in pMOS devices the active defect density is approximately 10 times larger than in nMOS,[10] BTI is typically considered more important for pMOS transistors. Nevertheless, for CMOS applications BTI of both device types is of significant importance, and the understanding of the physical origin of charge trapping in these devices is vital for further optimization of devices and circuits. Critical questions in this regard are the magnitude of the trap density, the impact of a defect on the overall device performance, and also the trap distribution and the trap levels. The most accurate way to answer these questions is by performing a detailed single-defect study employing nanoscale nMOS devices to provide the missing information.

Experimental: In contrast to large-area devices, the recovery in nanoscale transistors after PBTI stress proceeds in a discrete manner, see Figure 1. The recovery traces are typically given in terms of an equivalent shift of the threshold voltage $\Delta V_{\rm th}$, which is obtained by mapping the measured drain current using an initial $I_{\rm D}(V_{\rm G})$. To achieve highest measurement resolution for single charge transitions of $\Delta V_{\rm th} < 1\,{\rm mV}$ for the investigated SiON nMOS devices (W=90 nm, L=70 nm) we use our optimized defect probing instrument.[11] This enables us to observe a number of electron emission events (Figure 1 (left)), but quite remarkably also a significant number of hole traps with steps in the opposite (positive) direction, see Figure 1 (middle). In contrast, no electron emission events are visible in the recovery traces measured from pMOS devices of similar geometry, see Figure 1 (right). While the lack of observable electron trapping in pMOS devices may be due to the higher noise level, the presence of electron and hole trapping in nMOS devices signifies an important difference between NBTI and PBTI.

Defect Distribution Function: To study the relative contribution of electron and hole trapping to $\Delta V_{\rm th}$, the complementary cumulative distribution function (CCDF) of the absolute value of the step heights of 79 nMOS transistors of the same technology is evaluated, see Figure 2. The shown CCDF shows a weak bi-modal behavior, which can be separated into two (nearly) unimodal distributions, which can be attributed to hole and electron traps. Considering the trap density, a remarkable number of 106 defects (38%) are identified as hole traps among a total number 266 traps. The absolute contribution of hole traps to $\Delta V_{\rm th}$ is analyzed in Figure 3, and we observe that hole trapping decreases the total $\Delta V_{\rm th}$ by about 22% for the bias and temperature conditions used here. This finding suggests that hole trapping plays an important role in the context of PBTI.

Of further interest is that the significantly smaller step heights for hole traps compared to electron traps observed from the CCDFs, give rise to the assumption that hole traps might be located at a distance to the channel while electron traps reside closer to the channel. To settle this question the charge trapping kinetics of a number of hole and electron traps is evaluated next.

Single Defects: In order to study the charge capture and emission times, as well as their bias and temperature dependence, of single-defects we employ the TDDS.[2] To extract the charge emission time, stress ($V_{\rm DS}$=0 V, $V_{\rm G}$=$V_{\rm G}^{\rm s}$) and recovery ($V_{\rm DS}$=0.1 V, $V_{\rm G}$=$V_{\rm G}^{\rm r}$) cycles are repeatedly applied, and the recovery behavior is measured. During one measurement series typically 100 traces are recorded at the same bias and temperature. Afterwards the discrete steps of the $\Delta V_{\rm th}$transients are extracted, and the emission time is calculated as the average of all single emission events of a certain defect, see Figure 4. In one of the DUTs we identified three electron traps with negative step heights (Figure 5), and another device we observed two hole traps with a positive step height (Figure 6). For electron and hole traps we observed that with increasing device temperature, the clusters move towards shorter emission times. This observation confirms previous findings that both electron and hole trapping are temperature-activated processes.[2,9,12]

Results: In the following we evaluate the trap depth and trap levels of our defects. Previous reports have demonstrated that there is a direct correlation between the slope of the CCDF of step heights and the trap depth ($\eta \propto x_{\rm T}$).[9,13] However, from TDDS experiments it has been observed that defects can change their contribution to the threshold voltage shift when the device electrostatics at which the recovery is recorded changes.[9,14] As such, the step height alone is not a reliable indicator for the trap depth. To achieve an accurate estimate for the trap position inside the band diagram we evaluate the charge trapping kinetics of three hole traps (Figure 7) and nine electron traps (Figure 7) by employing a two-state defect model.[15–18] The estimated trap positions and trap levels for the analyzed traps are collected in the band diagram in Figure 9. A necessary condition for a defect to contribute to $\Delta V_{\rm th}$ is that the defect must be energetically located in the active region for charge trapping, which is observed for all single-defects. While the positions of the electron traps are found to be closer to the channel, the hole traps tend to reside in the middle of the insulator. Note that, in accordance to the defect model, the spatial position is mainly determined by the gate bias dependence of the charge capture time. The observation that hole traps with smaller step heights are found distributed at a distance from the channel is fully consistent with the average step height extracted from the CCDF of step heights.

Finally it is worth mentioning, that the trap levels of our study are in good agreement with DFT calculations suggesting that the oxygen vacancy is a potential trap candidate for electron trapping.[19,20]

Conclusions: By studying PBTI at the single-defect level in SiON nMOS devices we have observed charge trapping of electron traps in addition to a sizable number hole traps. Furthermore, we observe a bi-modal step height distribution which can be separated into two nearly uni-modal distributions, one corresponding to hole traps and the second one to electron traps. Our study clearly reveals that about 40% of the observed defects are hole traps, with are responsible for about 20% of the overall device degradation. The presence of electron and hole traps is a significant difference to the NBTI case. To extract trap parameters we study the charge trapping kinetics of a number of hole traps and electron traps, which we explain using a two-state model. The obtained trap parameters indicate that hole traps reside more likely in the middle of the insulator, while electron traps are more likely located near the channel. Finally, the calculated trap positions and trap levels lie inside the active energy region for charge trapping of the band diagram of the nMOS transistor, and are fully consistent with trap levels for electron and hole traps extracted from DFT calculations.

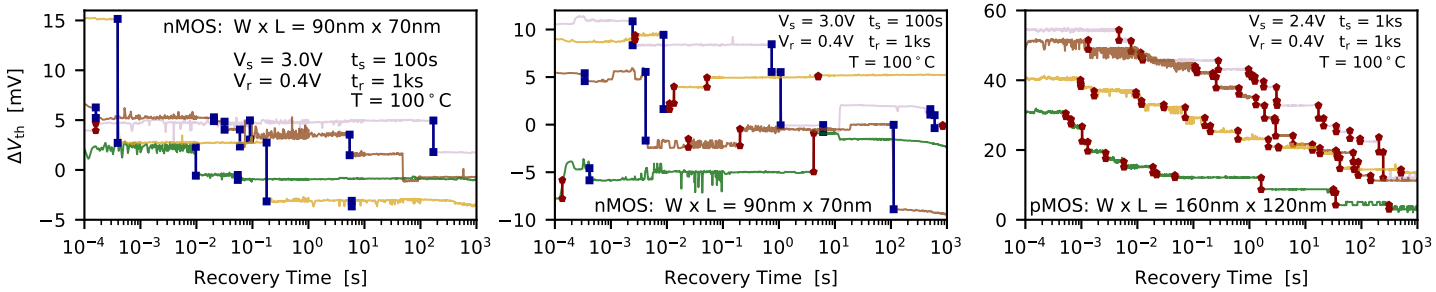

Figure 1: Selected recovery traces of several planar n-channel MOSFETs recorded after PBTI stress clearly show electron emission events (blue) with negative steps (left) and also hole emission events (red) with positive steps (mid). For comparison, the recovery traces of planar p-channel MOSFETs of comparable geometry (right) show many more steps and noise, which is due to the higher trap density compared to their n-channel counterparts. Note that the discrete steps originating from noise and RTN are not marked in the traces.

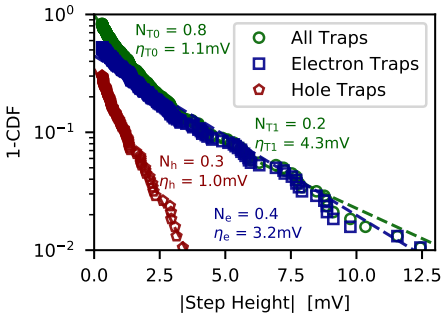

Figure 2: The step height distribution of planar n-channel MOSFETs. The distribution function of all steps appears to be bimodal. The bi-modal distribution can be separated into two (nearly) exponential distributions attributed respectively to hole and electron traps.

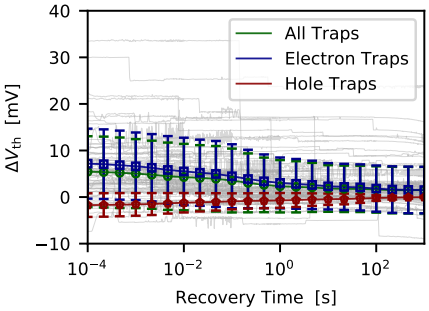

Figure 3: The average recovery behavior for nMOS transistors is calculated from the recovery traces (light grey) which are used to create the CCDF, see Figure 2. The major contribution to the threshold voltage shift originates from electron traps, but there is a sizable reduction of about 20% due to hole trapping to PBTI.

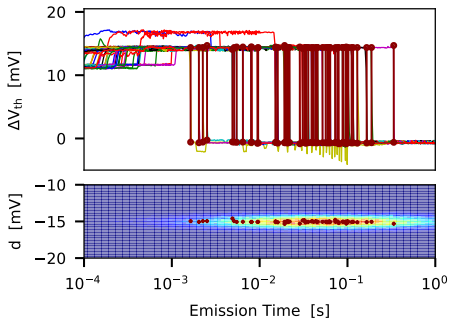

Figure 4: By repeatedly applying stress and monitoring the recovery behavior afterwards, the charge transistion events of a single defect can be recorded. These steps are extracted and binned into a histogram, called the spectral map. The charge emission time is given by the mean time of all emission events at a given bias and temperature.

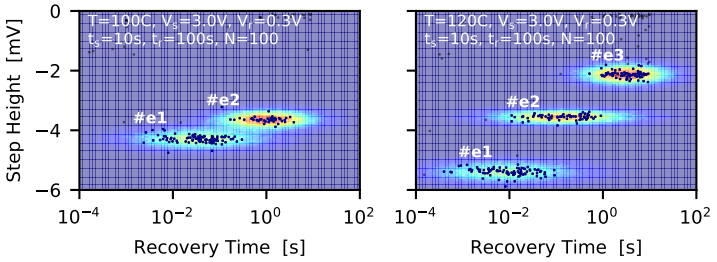

Figure 5: The spectral maps for one device at two different temperatures demonstrate the temperature dependence of several properties of particular defects represented by the clusters. For this device three electron traps with negative step heights can be observed.

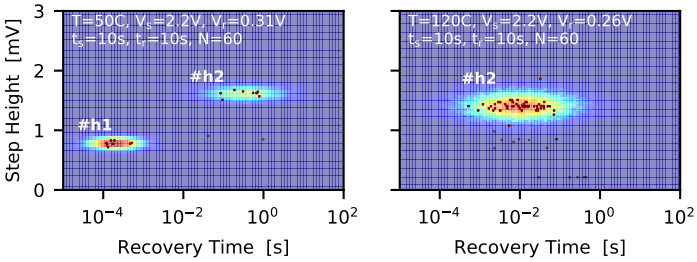

Figure 6: Similarly to the electron traps, the two hole traps #h1 and #h2 with positive step heights move towards lower emission times with increasing temperature. Defect #h1 is shifted out of the measurement window when the device temperature is increased by 70 °C.

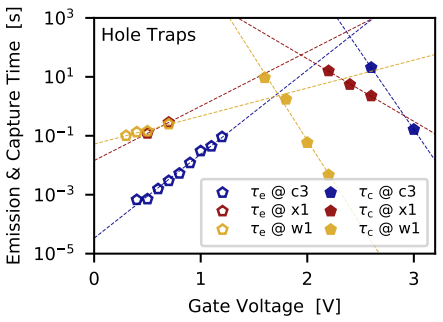

Figure 7: All measured charge emission and capture times from hole traps (symbols). The charge transition times are fitted using a two-state trapping model (lines).

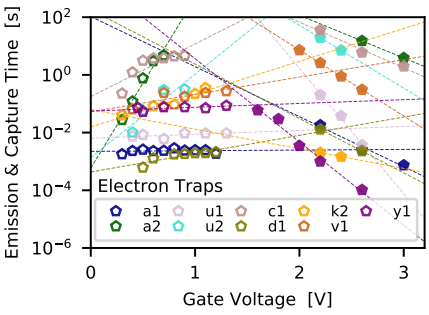

Figure 8: Charge capture emission (open symbols) and capture times from electron traps (filled symbols). The measured behavior can be nicely described by the two state model over a wide bias range.

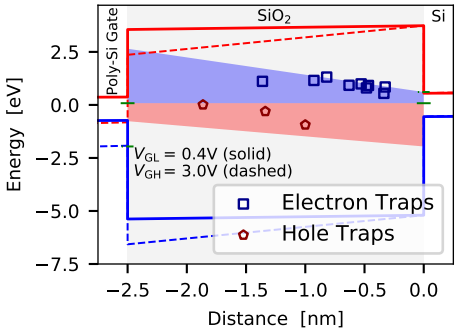

Figure 9: The band diagram shows the trap positions and trap levels extracted for single electron and hole traps. All identified traps are located in the active energy region for charge trapping (green), confirming the accuracy of our study.

References

[1] R. Wang *et al.*, *IPFA* (2018). [2] T. Grasser *et al.*, *IRPS* (). [3] T. Grasser *et al.*, PRB **82**, (2010). [4] B. Kaczer *et al.*, *IRPS* (2009). [5] H. Reisinger *et al.*, T-DMR **7**, (2007). [6] J. P. Campbell *et al.*, *IRPS* (2009). [7] T. Nagumo *et al.*, *IEDM* (2009). [8] D. Veksler *et al.*, *IRPS* (2013). [9] M. Toledano-Luque *et al.*, ME **88**, (2011). [10] M. Waltl *et al.*, *IRPS* (2014). [11] M. Waltl, T-DMR (2020). [12] H. Reisinger *et al.*, *IRPS* (2006). [13] A. Ghetti *et al.*, *IEDM* (2008). [14] A. Asenov *et al.*, T-ED **50**, (2003). [15] K. S. Ralls *et al.*, PRL **52**, . [16] M. Kirton *et al.*, Adv.Phys. **38**, (1989). [17] T. Nagumo *et al.*, *IEDM* (2010). [18] B. Stampfer *et al.*, MDPI Micromach. (2020). [19] A.-M. El-Sayed *et al.*, PRB **89**, (2014). [20] A. Kimmel *et al.*, *ECS T.* (2009).