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Abstract:
The main objective of this work is to suggest an FIR filter for convolution based DWT in image processing. Image processing using filters mainly suffer from the delay caused by the multiplier unit. Here with we have proposed Booth multiplier based MAC architecture for the design of FIR filter. Hence the overall system achieves and maximum speed improvement of 13.83% and area reduction by 22.39%. This work assures that the performance improved VLSI architecture for image processing with DWT techniques.

Keywords: FIR Filter,DWT image processor,Multiplier

Introduction:

Recent days the usage of DWT based image processing is of the essence in reducing the storage space needed for an image. This also can be enhanced by many different compression techniques. But the resultant image may not have higher order of reduction. But by using DWT scheme the order can be improved up to the level of 1/N, where the N is the number of quadrants (LL, LH, HH, HL).

While performing the wavelet compression, the invisible high frequency, high resolution part of images can be neglected [1]. This will makes the compression as most efficient one, as the ¼ of the image only used to store. A convolution based 3 level architecture is also proposed in [2]. However the 2 level itself a popular technique to produce compact image.

High throughput and less computation time applications can be opt for this architecture, which reduces the computation time by half. Also the lifting base structures save considerable area. The Two dimensional multi level DWT is discussed in the paper [2] and the extended the same up to the dimensions of three using bi-orthogonal and Daubechies filters.

The line buffered wavelet filer having M as the number of image proposed in [2] has the benefit when it is used in top throughput. This leads to the drawback of having more adders and multipliers. If there is more mutual architecture available which computes data streams, then 100% hardware utilization is possible [3].

1.BOOTH MULTIPLIER BASED FIR:

Booth multiplier-based product generation has the advantage that the number of partial product rows required to calculate the product will be exactly half that of number of partial products needed for the ordinary multiplication methods. For an example the number of partial product rows needed for 64 bit ordinary multiplier is 64 rows, wherein the same multiplier would generate only 32 rows in the case of booth based techniques. An example for booth multiplier was shown in figure 1. Here 6x6 bit multiplications were performed. But instead of producing 6 PPR rows, only 3 rows were generated to produce the product values.

						0	0	1	1	1	0	Multiplicand
						0	1	0	1	0	1	Multiplier
0	0	0	0	0	0	0	0	1	1	1	0	PPR 1
0	0	0	0	0	0	1	1	1	0	0	0	PPR 2
0	0	0	0	1	1	1	0	0	0	0	0	PPR 3
0	0	0	1	0	0	1	0	0	1	1	0	Product

Figure 1: Example 6x6 Booth Multiplier

This makes the number of multiplier component will be reduced in numbers and there by the architecture size reduced [4][5].

2.FIR FILTER:

The filters are playing important role in selecting the required value from the large numbers. Here in the case of DWT as a compression technique, only the most important information alone to be taken for defining the images. The high frequency values will be neglected while the picture is being compressed.

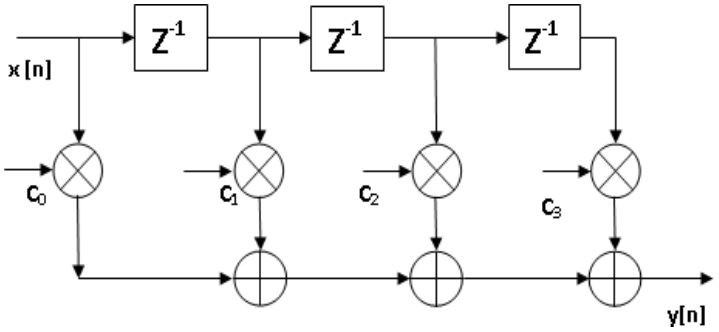


Figure 2: A simple FIR filter structure

For selecting the low frequency values from the available image samples, the FIR filer is used. A simple FIR filter structure is shown in figure 2. So this filter also called as low pass FIR filter in DWT process.

3.DWT SYSTEM:

The Image compression techniques can be split into two types, known as Lossy compression and Lossless compression. Further the Lossless compression has Entropy coding and Decorrelation technique.

The RLC and Statistical codes falls under the category of Entropy coding, wherein the prediction-based compression, Transform-based compression and Multi-Resolution-based compression are the types under the category of Decorrelation method.

On the other hand, the lossy compression technique has transform-based and Non-transform based compression as types. Vector quantization and fractals are the types of Non-transform based compression techniques.

The advanced and high efficient compression techniques like DCT and DWT falls under the category of Lossy-transform-based compression techniques. The DWT removes the drawback of DCT.

A Wavelet is a function which has the properties like average value as 0, duration limit and frequency varying, with waves on the top and underneath the x-axis. Sometimes high frequencies uses narrow windows and low frequencies would be preferred at wider windows. A wavelet is like sin and cos functions with $\psi_k(t)$ function as given below

$$f(t) = \sum_k a_k \psi_k(t)$$

A full image will be applied to DWT compression process. So that better compaction in energy is achieved as compared to DCT techniques. There are four sub bands available in terms of frequency as shown in table 1.

Table 1: Sub Bands of DWT

Frequency band	Horizontally	Vertically
LL	Low pass	Low pass
LH	Low pass	High pass
HL	High pass	Low pass
HH	High pass	High pass

Usually a low pass filer will be used as FIR filter, and the image is passed in it. The undisclosed information of the images will be put out of sight in the LH, HL & HH portions and only LL portion of Low frequency image element is more perceptive to our human eyes. It is obvious that the disclosed information in three portions has no data in it and this high frequency parts will not affects the quality of the image [6].

Three more important properties are Linear-time complexity, Adaptability and Sparsity. In special case of finger print image compression, image fusion, Image matching and retrieval, image recognition and Noise filtering the wavelet compressions can be applied [7, 8].

3.1CONVOLUTION BASED DWT SYSTEM:

The Multiply and Accumulation unit is a heart of FIR filer design. This MAC unit has multiplier and accumulators [9]. The multipliers produces product for floating point input numbers. The addition process repeated every time to add the product with the previous MAC output. This can be given by the equation,

$$m[i] = m[i-1] + x[i].y[i]$$

where m[i] is the MAC output at i^{th} iteration, x[i] & y[i] represents the input for the multipliers. Here instead of ordinary multiplier, booth multiplication is used to generate the products, so as to minimize the number of partial product rows. Solo stage pipelined 8 bit floating point filter structure is shown in figure 3.

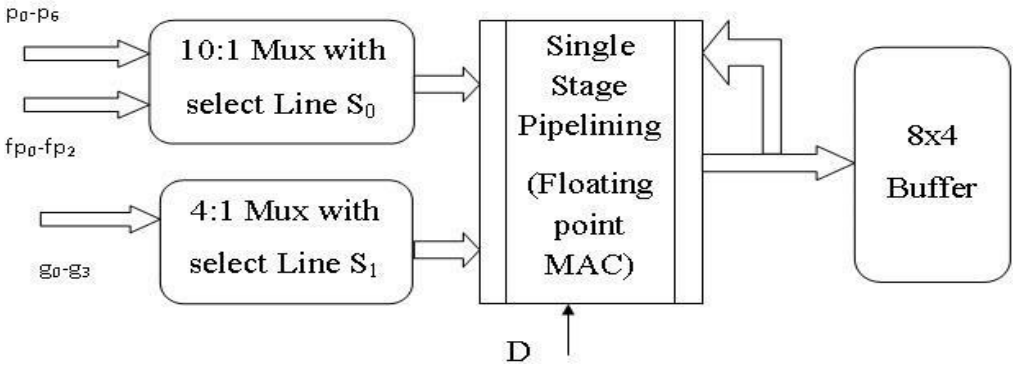


Figure 3: Single stage pipelining structure

Input bit D decides the type of operation performed. If D=1, then it performs multiplication and if I is 0 then MAC operation is performed. Select line decides the input to be passed through it during the row and column processing. Totally 96 clock cycles needed to complete the row processing. Number multiplicands will decide the

number of clock cycles. By using pipelined structure with two MAC units, convolution time can be reduced by half and requires small area and very small power consumption for the operations.

4.MODEL FOR DWT IMPLEMENTATION:

HDL codes for both existing and proposed designs are modeled and simulated in Xilinx ISE simulator and by Cadence tool the codes were synthesized. In the overall architecture shown in figure 4,

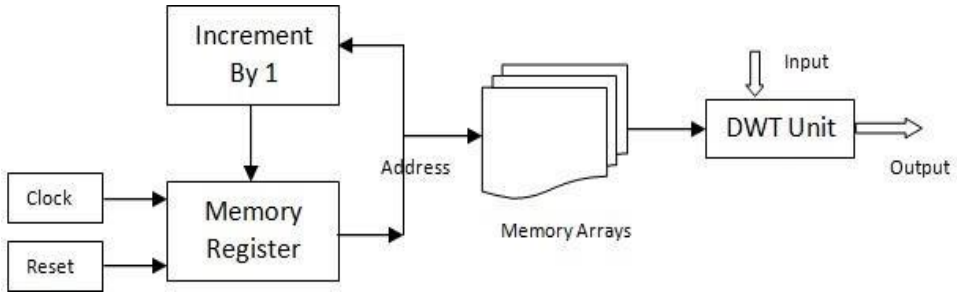


Figure 4: Overall architecture of DWT

Proposed DWT gets the selected address lines from the lookup table, where all the sect lines are being stored. A preset register operated by means of clock will be continuously incremented by the Adder with default '1'as one of the input. This will help the address lines of be continual values are stored in lookup table.

The DWT of the image is obtained by using direct DWT2 function in matlab code [10]. The same can be obtained by using the DWT algorithm, which is explained in this section.

The algorithm setup can be written in Hardware Description Code. The HDL code again simulated in Xilinx tool to verify its functionality, and the same can be used with the booth multiplier instead of the ordinary multipliers.

Here the number of partial product rows can be minimized into half of the actual no of rows required. This will be an added advantage for the area wise reduction of the architecture and speed of the circuit can also be improved to better extent.

Again the HDL code with booth multiplier for the DWT was simulated to get the DWT transformed image. This can be extended up to N number of dimension as like matlab code does. The extended dimensions like 2D and 3D DWT also possible with this technique, finally the proposed architecture is implemented in the FPGA kit and the performance analyses were done.

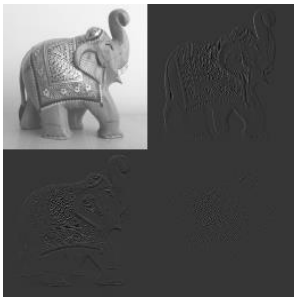
5.SIMULATION RESULT ANALYSIS:

The simulation result shows that the PSNR values are high and the pictures looking same as other compression techniques. The simulations were done by using matlab software. Also the VHDL simulation was done by using model sim and the parameters evaluation s carried out by cadence software.

The mean square error (MSE) is given by, $MSE = \frac{1}{L}\sum_{i=1}^{L}[p_i - q_i]^2$ Where the input sequence is p_i, output sequence is q_i, and data sequence length is denoted by L. Also the Pixel to noise ratio is given as,

$PSNR = 10\ log_{10}\left(\frac{p^2}{MSE}\right)$ where p is the peak value of the input sequence.



(a) (b) (c) (d)

Figure 5: (a) & (c) Original Images, (b) & (d) DWT image

5.1TABLES & GRAPH:

The area and delay values for different compression techniques were shown table 1. It is observed that the performance of the dwt is more suitable for the image processing where there is a lack of storage space with improved performances as tabulated below.

Table 2: Performance analysis

Methods	Area (µm2)	Delay(ps)
Floating point DWT in [11]	52678.3	26479.2
Floating point DWT in [12]	29458.1	27968.4
Floating point DWT in [13]	58945.6	253147
Proposed DWT	**45746.2**	**24569.2**

Average performance of the proposed technique satisfies the significant reduction in both area and delay values as shown in figure 6&7.

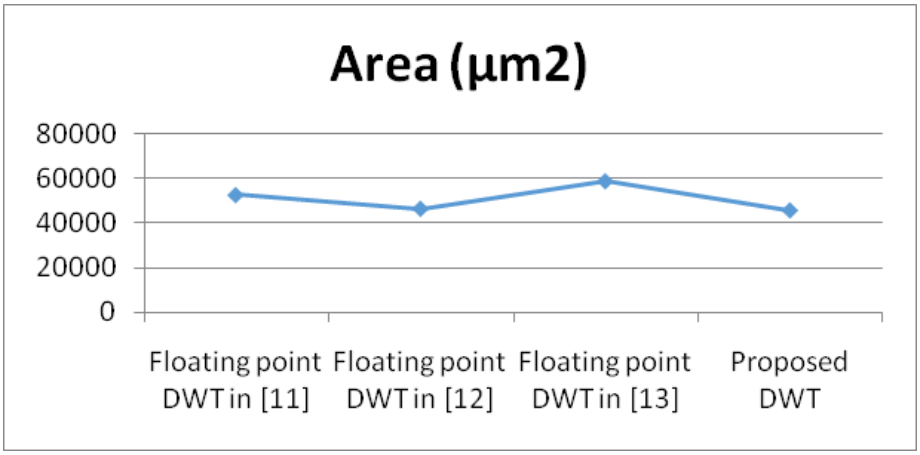


Figure 6: Area comparison

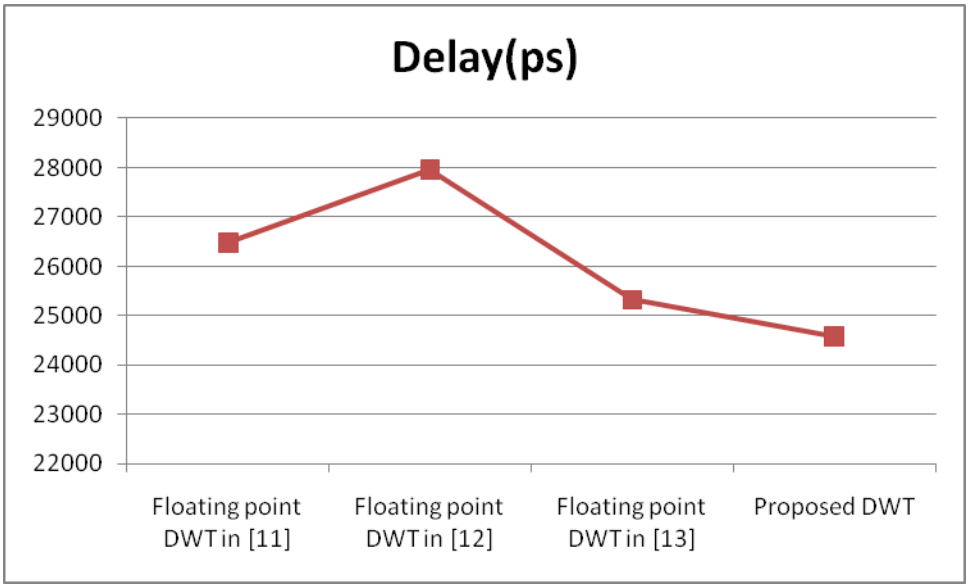


Figure 7: Delay comparison

RESULTS AND DISCUSSION:

The Result shows that the proposed work and the existing work will produce same image output. But the performances wise, area utilization wise the proposed architecture stands in its place. So this proposed architecture can be used in DWT based image processing applications like convolution based compression with minimum number of resources, energy and time.

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