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Comparison of 4 bit adders in CMOS and GDI logic

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Comparison of 4-bit Adders in CMOS and GDI Logic

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***Abstract*—Circuit Performances in VLSI technology always depends up on the individual processing elements and the interconnections in the circuit. Adders are the key elements in all digital systems which perform addition of numbers. Here this work focus on performance comparison of existing CMOS logic and new GDI(Gate Diffusion Input) technology by designing 4-bit adders such as Ripple Carry Adder (RCA), Carry Save Adder (CSA) and Carry-lookahead Adder (CLA). Performance analysis of adders is presented with respect to layout area, transistor count, number of devices and delays are discussed. All adders are designed using Tannerv15.2 with 180 nm technology. Simulation results shows that proposed GDI 4-bit adders are more efficient in terms of area and delay when compares to CMOS logic.**

I. INTRODUCTION

Today most of the processors require a very high-speed operation. Performance of any circuit can be analyzed by using speed and delay factors. To speed up the process in various digital circuits, arithmetic operations such as addition, subtraction and multiplication are used. There is a high demand for high performance and low area integrating circuit design in advanced electronics and communication technologies. Arithmetic logic unit (ALU) is the main component in any circuits and networking protocols.

Addition is the massive operation in most of the processors. Adders are the basic building blocks of many architectures so in this context approximate adders are introduced which can reduce complexity of the hardware and gives efficient energy compared to other adders. 1 bit full adder gives sum of 3 inputs and a carry value.

In CMOS VLSI design approximate computing (AC) emerged as a promising technic to drive energy and efficiency. It can trade of balance between accuracy vs performance/power.

Here, we are using three adders which supports multiple bits are Ripple carry adder (RCA), carry save adder (CSA), carry lookahead adder (CLA).

Gate diffusion technic (GDI) was proposed by Morgonshtein et al. It is used for designing of low power circuits which reduces power consumption, area and propagation delay. A different adder was proposed to satisfy the increasing demand such as CSA, CLA and RCA using GDI technique that reduces the area and delay when compared to CMOS based designs.

II.BACKGROUND

A. Ripple Carry Adder

Ripple carry adder is a combinational logic circuit and a type of digital adder used to compute the sum of two n-bit numbers. It contains combination of n number of full adders according to the no of input bits used. Here each carry bits gets rippled in to next stage.ie carry out generated by a full adder serves as carry -in for its next full adder. It does not allow to use all full adders simultaneously. RCA can be also called as n-bit parallel adder. Fig 1 shows the block diagram of RCA adder.

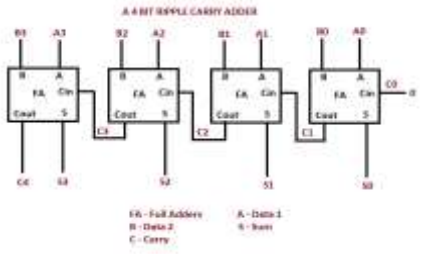

Fig 1: block diagram of RCA adder

B.Carry save adder

Carry save adder (CSA) is a type of digital adder which is used to compute the sum of three or more n-bit numbers. CSA is a combination of full adders and half adders depending on the number of bits added. It gives output as two numbers one is set of sum bits and other set is carry bits. so an n-bit CSA receives 3 n-bit inputs, i.e. x(n-1)….x(0), y(n-1)….y(0), and z(n-1)…z(0) and makes two results sum and carry of n-bit, i.e. Sum(n-1)…Sum(0) and Carry(n-1)….Carry(0) . then, it can be also called as (3, 2) counter. Figure (2) shows the block diagram representation of a carry save adder.

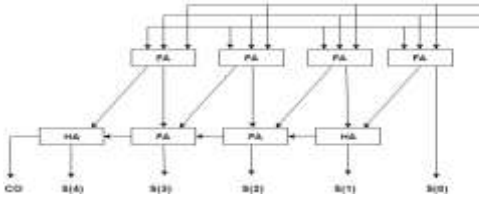

Fig 2: block diagram of CSA adder

C.Carry Lookahead adder

A carry-look ahead adder (CLA) also called as fast adder is a type of electronics adder used in digital logic. CLA increases the speed by reducing the time taken to determine carry bits [2] .The CLA finds further carry bits before the sum. So it can reduce the time taken to calculate the output of the adder which has large value bits [3]. Sum of each bits are designed for each bit by getting carry value from the previous bits. CLA uses the concept of generating and propagating carries. Fig 3 shows the block diagram representation of carry look-ahead adder.

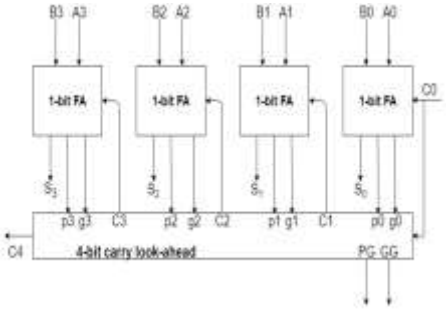

Fig 3: block diagram of CLA adder

III.GDI TECHNIQUE

Gate diffusion input (GDI) is a technique used for designing of low-power digital combinatorial circuits. Area of complexity, propagation delay and Power consumption are reduced using this technique by reducing the number of transistors in the circuits, thereby it can maintains low complexity in logic design [5].The GDI method is implemented using two transistors for a deep range of multipart logic design. This method is suitable for the structure of fast and low power circuit and small area needed circuits

The basic structure of the GDI resembles similar to the structure of the CMOS inverter, but there are some main differences: The GDI basic cell consists of 3 inputs: G (common gate input of nMOS and pMOS), P (input to the source/drain of pMOS), and N (input to the source/drain of nMOS). 2) Bulks of both nMOS and pMOS are connected to N or P (respectively), so it can be arbitrarily biased at contrast with a CMOS inverter. Fig 4 shows the basic GDI cell.

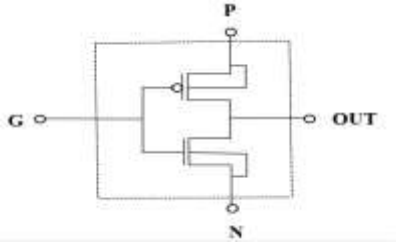

Fig 4: basic GDI cell

By using GDI design any complex function can be make simple when compared with CMOS based design and standard PTL [4][5]. In GDI implementation of the OR, AND gate requires two transistors and OR gate require four transistors. While noticing the growing challenges of the digital design it seems to be that GDI technique is more suitable when compared to other techniques. So this method is easy to implement, cost effective and are depends on multi-functional building blocks [6]

IV.PROPOSED DESIGN

Here, the performance and analysis of various adders using GDI technique has been presented and simulation is done. The adders executed using GDI method are ripple carry adder (RCA), carry save adder (CSA) and carry-lookahead adder (CLA).

A.Ripple Carry Adder

A Ripple carry adder is a concatenation of full adders. Here each carry out is rippled to the next full adder as inputs. It is one of the most compact adders which can be used to design compact adders. By the GDI design we can reduce the area of the RCA and can reduce propagation delay. GDI based RCA adder design diagram is shown below in the fig 5.

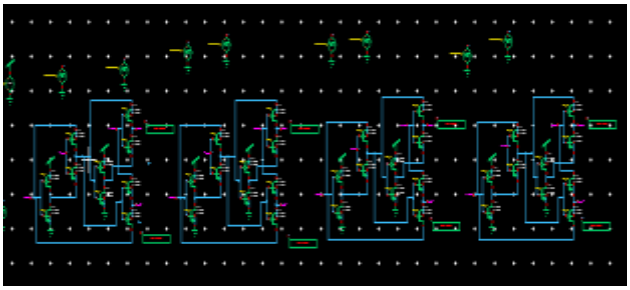

Fig 5: Schematic of GDI based Ripple carry adder

B. Carry Save Adder

Carry Save Adder (CSA) implements the synchronous adder of various operands [3]. It is used in different computer architecture for finding the summation of n-bit numbers and giving output as sum and carry of these input bits. Using this GDI technique, it can reduce transistor counts and the area of complexity [8].The schematic representation of GDI based CSA is shown on figure 6.

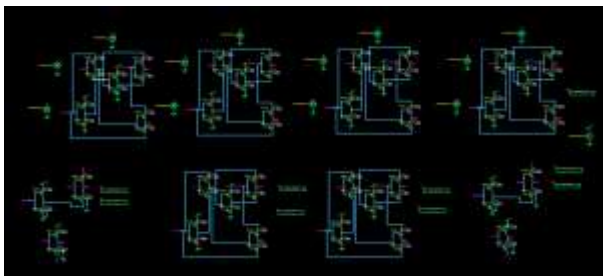

Fig. 6: Schematic of GDI based Carry Save Adder

C. Carry Look-ahead Adder

The carry-lookahead adder (CLA) determines the carry bits in advance thereby it reduces the propagation delay. This adder exhibits three stages a generate /propagation signal, a carry generator and a sum generator signal. Fig 7 shows the schematic diagram of GDI based Carry-lookahead adder (CLA).it is realized by the expression

Gi=AiBi for i=0, 1, 2, 3..etc.

Propagation signal can be realized using the expression

Pi=Ai;

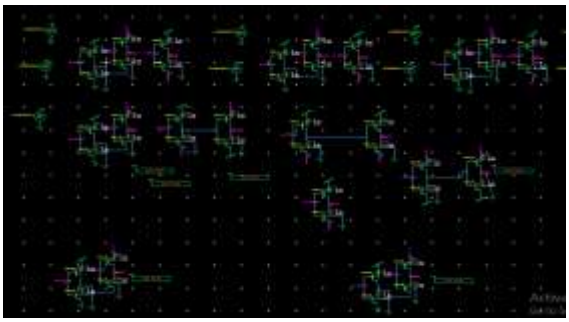

Fig. 7. Schematic of GDI based carry lookahead Adder

IV.SIMULATION RESULTS

In this section, the implementation and performance analysis of the proposed design are carried out. The analysis is observed at 250 nm technology using Tannerv.15.2. The performance of all the adders with the new GDI technique is determined in terms of transistor count and delay. Tanner EDA tools are used for building integrated circuits. These tools work on entering schematic, designing SPICE simulation, to do structural design and to do design rule checks (DRC) and layout versus schematic (LVS) checks. There are 4 types of tools in this process:

1. S-edit - a schematic tool
2. T-spice- simulation mechanism which is combined with S-edit
3. L-edit - a physical design tool to make layout
4. W-edit - the waveform tool

The adders are compared with both GDI and CMOS based technique which is shown in Table 1. From this table it is understood that the performance of the proposed GDI based circuits is better than the existing CMOS circuits according to reduced area and delay [10].

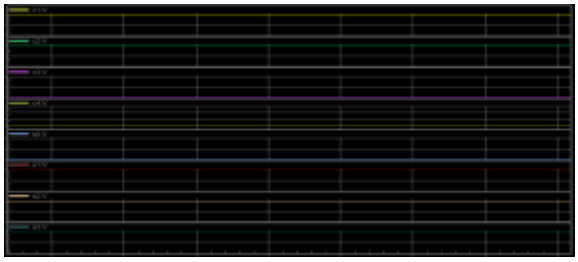

Fig 8: Output Waveform of GDI based Ripple Carry Adder

The output waveform of GDI based Ripple carry adder is shown in Figure 8. It is found that the noise margin is less, but when compared to carry look-ahead adder (CLA) it is more. In this scheme the output logics are set to logic 0 and logic 1 [11]. Here, three inputs are given for each bit they are X0Y0Z0, X1Y1Z1, X2Y2Z2 and X3Y3Z3 its outputs are Sum1, Sum2, Sum3, Sum4 and Cout.

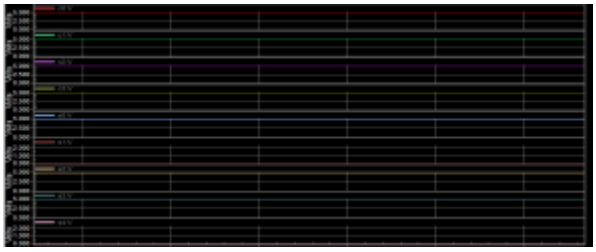

Fig 9: Output Waveform of GDI based Carry save Adder

The output waveform of GDI based Carry save adder is shown in Figure 9. It is observed that the noise margin is less, but when compared to carry save adder (CSA) it is more. In this scheme the output logics are set to logic 0 and logic 1 [11]. Here, three inputs are given for each bit they are A0B0C0, A1B1C1, A2B2C2 and A3B3C3. its outputs are Sum1, Sum2, Sum3, Sum4 and Cout.

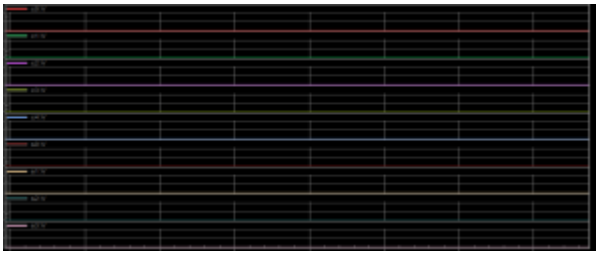

Fig. 10. Output Waveform of GDI based Carry lookahead Adder

The output waveform of GDI based Carry-lookahead adder is shown in Figure 10. It is noticed that noise margin is less but more when compared with proposed novel adder. In this system the output logics are set to logic 0 and logic 1. Here, two inputs are given for each bit, A0B0, A1B1, A2B2 and A3B3. The A and B values are given to XOR gate and AND gate so the outputs of it are propagating term P and generating term G. The output of the CLA is taken as S0, S1, S2, S3 and Cout.

Fig. 11 represents the graph regarding the performance comparison of both CMOS and GDI technique. From this Table 1 it is observed that proposed GDI based adders are faster and effective when compared to CMOS adders based on area of complexity and propagation delay.

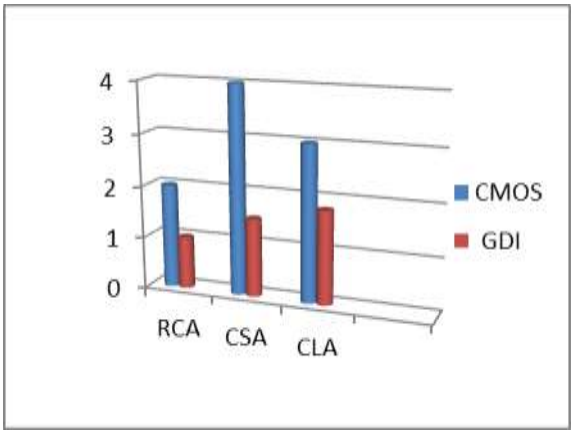

Fig. 11. Graph based on Performance Comparisons of GDI and CMOS

TABLE 1: PERFORMANCE COMPARISONS OF GDI AND CMOS ADDERS

Adders	CMOS			GDI		
	No. of Transistors	*Overhead Delay*	*Total Delay*	*No. of Transistors*	*Overhead Delay*	*Total Delay*
RCA	184	5.63 ns	8.1 ns	40	1.92 ns	2.11 ns
CSA	288	1.51 ns	4.61 ns	72	1.10 ns	1.31 ns
CLA	166	1.39 ns	1.69 ns	61	1.43 ns	1.59ns

From this table shown above it is clear that an adder designing based on GDI method is more efficient for today's challenging electronic circuits. Because this method is well suited for the low area needed circuits. It is a contribution to the integrated circuit designers.

V.CONCLUSION

The paper describes about the performance of various adders using GDI method and observed using tannerv15.2, using 180 nm technology. The parameters such as area, no: of transistors and overhead delay have been examined and compared with the existing CMOS logic method. The Adders using GDI technique performs well and better when compared with CMOS technique. Delay of the RCA, CSA and CLA using GDI method are reduced to 71.58%, 1.24% and 19.23% when compared to the exiting CMOS logic design. This technique can also use in multipliers to improve its efficiency.

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