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***Abstract*— With recent advances in Gallium Nitride (GaN) semiconductor technology, it is possible to achieve greater applications in the power electronics market, allowing high switching speeds and high power conversion densities by transistors. This work presents application of GaN transistors in the development of class D audio amplifier of 1KWrms in order to observe efficiency and losses generated in the switches, using complete bridge topology with unipolar modulation and proportional control integrative derivative (PID) digital. It obtains 97% yield on the amplifier and Total Harmonic Distortion (THD) of 0.23% through GaN transistor simulations and circuit simulation, in the prototype 97.7% of yield at maximum power are obtained.**

***keywords*——Class D Amplifier, GaN FET, GaN Transistor Losses, Hardware Simulation.**

I. INTRODUÇÃO

Power electronics over the years have made significant advances in the field of transmission and energy conversion benefiting several sectors. Since the development of class A amplifiers, new power technologies have been applied with the need to obtain greater potential and less waste in the conversion process, as well as the use of new topologies to achieve lower physical volumes of these equipments. With the demand for more powerful and compact audio amplifiers since their popularization in the 1980s and 1990s, different transistors were applied to amplifiers mostly Class B/AB, but always with significant losses and huge sinks [11].

As an alternative to Bipolar Transistors, the Semiconductor Metal Field Effect Transistor (MOSFET) of power first appeared in 1976. These devices were faster and more robust and had greater current gain, but other superjunction devices and the Isolated Door Bipolar Transistor (IGBT) have reached beyond the theoretical limits of a majority carrier mosfet, conductivity improvements, with this result the conversion of switching energy becomes a commercial reality [10].

Increasingly considered the viable semiconductor material in the future of power electronics, also called broadband semiconductors, The Gallium Nitride (GaN) is thus known due to the relatively large bonding energy of the atomic components in its crystalline structure. Although GaN is now establishing itself in the market they have already surpassed the feats of silicon semiconductors. With low Ron resistance and low gate loads and better reverse recovery, these features result in lower transistor losses, with greater efficiency at high frequencies [8].

The class D amplifier when proposed in 1958, had as theoretical objective to achieve 100% energy efficiency in the total modulation index, more due to losses inherent to the circuit components it was possible to obtain potentials higher than 90% yield where high efficiency requires good output inducers avoiding the propagation of switching frequency in the speakers [13], associated with this factor , the importance of using keys with lower losses shows an increase in the efficiency of projects in audio amplifiers [9]. The autor [4] states that once the potential for class D deficiencies are surpassed to pulse width modulation (PWM) amplification will be all that exists in audio equipment above 100w. This statement is already confirmed today with a strong presence of this technology, not only at high power but also in low power devices such as mobile phone, tablet and notebook [1]. This work aims to present the development of a class D amplifier of high power and efficiency with high frequency switching at 400 KHz using GaN transistors, with unipolar modulation, in a complete bridge topology with Inductive and capacitive filter (LC) Butterworth of 2nd order.

II. DEVELOPMENT OF THE CLASS D AMPLIFIER

A. Amplifier Topology

The proposed topology in Fig.1 of this project is based on a complete bridge voltage source inverter, in this application we have an Alternating Current (AC) output that is synthesized from a Continuous Current (DC) input voltage, not unlike the configuration of the digital amplifier, we have an AC output voltage and an audio sine input voltage connected to the comparator , a source of fixed bus voltage and at the exit a frequency variation between a range of 20Hz to 19KHZ in order to cover the range audible to the human being. The harmonics

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to be filtered in this topology are at high frequencies, also this topology allows working with various output filter structures, such as LC filters of 2nd order, LCL, LCLC, cascade and others.

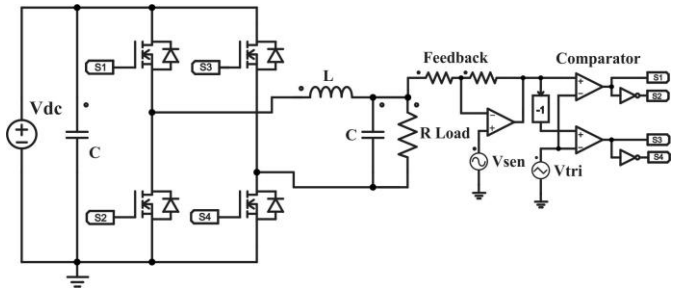

Fig. 1 Typical Circuit of an Inverter.

B. Modulation

The proposed modulation of the amplifier is the Unipolar Sinusoidal Pulse Width Modulation (SPWM) where the carrier is compared with the sinusoidal audio signal, this among others obtains a low total harmonic distortion (THD), enabling the quality of the audio signal played and lower losses in transistors. In the operating mode the output is switched in three levels, where the voltage varies from a high value to zero or from low to zero, different from bipolar modulation that only varies between two levels, being of high value to low. The switches on the two legs of the complete bridge are not switched simultaneously, the legs are controlled separately, comparing Vtri with Vsin and –Vsin as shown in Fig. 2.

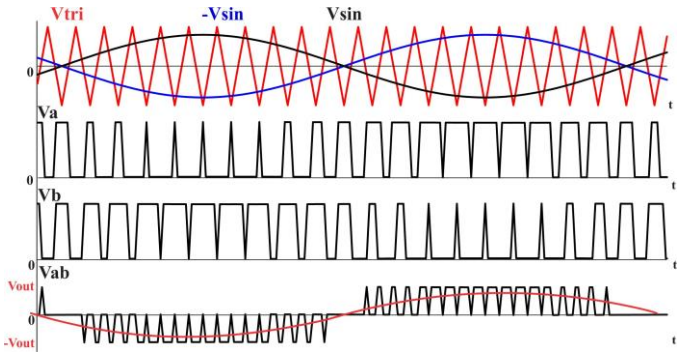

Fig. 2 SPWM Unipolar Modulation.

C. Amplifier Operation Steps

In this modulation we have eight stages of operation, four referring to the positive semicycle of the output voltage and four to the negative semicycle. Observing for the switches and diodes in this analysis that considered ideal we make analysis for only the positive semicycle where in the negative semicycle are analogous to the positive semicycle. In the first stage of operation in Fig.3 we have the S1 and S4 switches conducting load current. In the second stage of operation we have the S4 transistor in lock in time t1 enabling the Diode D2 to enter into driving, which due to the direction of the current the S2 transistor does not drive, even with the command in t2, thus has a free wheel in the load. In time t3 the Switch S2 is locked and we have in t4 the S4 switch again commanded to drive, where is assumed the current circulating through diode D2. In the third stage we have the same operation as in the first stage. In the fourth step the S1 switch has the lock on t5 with the D3 diode going into operation assuming the load current, although commanded at t6 the S3 switch does not reach drive, due to the direction of the current. In t7 the S3 switch is locked and in t8 the S1 switch is commanded to drive this assumed the current circulating through the D3 diode, ending the positive semicycle and returning to the first step [6]. The steps and switching time are presented in Fig. 3 and 4.

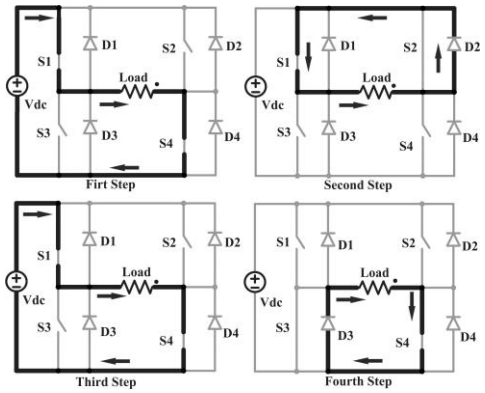

Fig. 3 Converter Operation Steps.

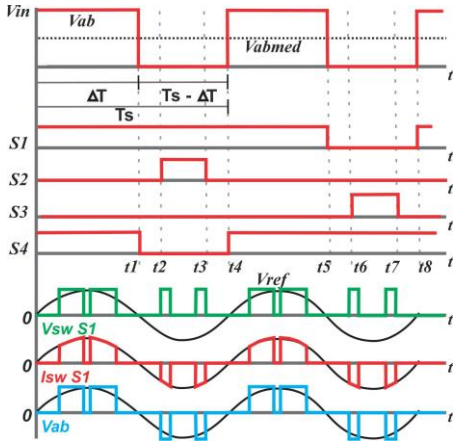

Fig. 4 Switching times on the switches, voltage, current and output voltage.

D. Instant Average Duty Cycle

In sinusoidal PWM we have the duty cycle calculated using two switching periods due to the modulation employed. We then analyzed the modulation compared with Vtri which in this case has two Vcontrol signals crossing the triangular signal, with this the mean duty cycle is presented for several modulation indexes in (1), Where α is the angle between voltage and current of the load that in this project is considered, only a resistive load. m_a is the modulation index given by (2) which is the rate of the amplitudes of the reference signals.

$$D(t) = \frac{1}{2}\left(1 + m_a \cdot \sin\left(\omega t + \alpha\right)\right) \quad (1)$$

$$m_a = \frac{V_{o\_pico}}{V_{dc}} = \frac{V_{control}}{V_{tri}} \quad (2)$$

Amplitude modulation has an important function in the amplifier because if m_a is less than or equal to the amplitude of the fundamental frequency of the voltage in the output, V_{ab} is linearly proportional to m_a, this means that we can have a volume control at the exit of the signal with respect to the input signal and also allows that when there is a power voltage V_{dc} which is the unregulated bus voltage, m_a can be adjusted to compensate for these variations in DC power voltage [7].

E. Voltage and Current in Load

Equation (3) and (4) represents the waveform of the voltage and currentin in the output terminals $V_{ab}1$ representing the fundamental frequency component in the positive semicycle of the output voltage.

$$V_{ab1} = m_a \sin(\omega_1 t)\ ,\ \text{com}\ m_a \leq 1.0 \tag{3}$$

The output current is given by (4) for a resistive load.

$$i_{out}(t) = I_{o\_peak} \sin(\omega_1 t) \tag{4}$$

F. Harmonics

In unipolar modulation, it is noted that the number of pulses in vab voltage is twice as high in modulation of three levels than that found in the modulation of two levels, for the same frequency of switching. This number is directly related to the frequency of V_{ab} harmonics. The advantage of "effectively" duplicating the switching frequency appears in the harmonic spectrum of the output voltage waveform, where the lower harmonics appear as side bands of twice the switching frequency. In [12] we see that the wave-shaped harmonics of the inverter output voltage appear as side bands centered around the switching frequency and its multiples, i.e. around harmonics, m_f, $2m_f$, $3m_f$ and so on. This general pattern is valid for all values of m_a in the range from 0 to 1. Theoretically the frequencies at which the voltage harmonics can be indicated is given by (5) and (6).

$$f_h = (jm_f \pm k) f1 \tag{5}$$

Where *h* is the harmonic order corresponding to *k* side bands and *j* is the modulation frequency m_f.

$$h = j(m_f) \pm k \tag{6}$$

Where the fundamental frequency corresponds to *h* = 1. For odd values of *j*, harmonics exists only for peer values of *k*.

G. Control Technique

The control circuit used in the project is the voltage mode, seeking in this to minimize the effects of the intrinsic nonlinearities of class D amplifiers that incurs many distortions and electromagnetic noises. Thus, a control is necessary that can minimize such effects and ensure that the circuit responds by a certain frequency band. To reach the mathematical model of this Class D amplifier, it is considered its main operating characteristic that has the ratio of the output voltage by the input voltage determining its respective input gain at the output. For this we model using the PWM switching model, to control a function involving the output voltage in relation to the modulation function, this is because the amplifier must receive a variation of frequencies and amplitudes of the audio signal.

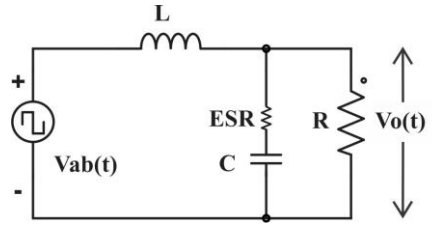

Fig. 5 Electrical scheme to obtain the transfer function.

H. Loss in the Transistor GaN

This section presents the loss measurement elements in the GaN transistor in order to obtain losses by switching, reverse conduction and direct driving losses.

I. Switching Losses

The autor [2] states that switching losses are responsible for most losses and is an important charge of device power. It is considered the losses by transition (Turn-on and Turn-off). The equations associated with these losses are given by (7) and (8) for the ascent time and (9) and (10) for the downtime on and off for the transistors.

$$t_{cr} = \frac{Q_{oss_{Q2}} \left(R_{G_{\text{int}}} + R_{G_{ext}} + R_{pu} \right)}{V_{drv_{on}} - \left(\frac{V_{GS_{(th)}} + V_{PL}}{2} \right)} \tag{7}$$

$$t_{vf} = \left(\frac{Q_{oss_{Q1}} + Q_{oss_{Q2}}}{V_{drv_{on}} - V_{PL}} \right) \left(\frac{1}{g_{fs}} + \frac{2(R_{G_{\text{int}}} + R_{G_{ext}} + R_{pu}) C_{RSS_{Q1}(0V)}}{C_{oSS_{Q1}(0V)} + C_{oSS_{Q2}(V_{dc})}} \right) \tag{8}$$

$$t_{cf} = \frac{Q_{oss_{Q2}} \left(R_{G_{\text{int}}} + R_{G_{ext}} + R_{pu} \right)}{\left(\frac{V_{GS_{(th)}} + V_{PL}}{2} \right) - V_{drv_{off\,(0V)}}} \tag{9}$$

$$t_{vr} = \frac{Q_{oss_{Q1}} + Q_{oss_{Q2}}}{IL_{turn_{off}}} - \frac{t_{cf}}{2} \tag{10}$$

Transistor switching losses on and off are given by (11) and (12) respectively.

$$P_{on} = f_{sw} \left(\frac{1}{2} V_{dc} \times IL_{turn_{on}} \right) \left(t_{cr} + t_{vf} \right) \tag{11}$$

$$P_{on} = f_{sw} \left(\frac{1}{6} t_{cf} \times IL_{turn_{off}} \times \Delta V_{dc\_cf} \right) \tag{12}$$

Where $R_{G_{int}}, R_{G_{ext}}, R_{pu}$, are the internal, external and *pull up gate* resistences, $V_{drv_{on}}$ is the drive voltage applied to the *Gate*, and V_{PL} is the voltage in the *Gate* when the transfer-source voltage transition occurs in the switching, $IL_{turn\_off}, IL_{turn_{on}}$ is the currents in the inductor for the on and off switch and ΔV_{ds_cf} represents the change in voltage during the transition.

J. *Reverse Conduction Losses*

Voltage drop and time can be calculated based on switching transition times. These on and off times are obtained from full load characteristics (Q_g) and can be obtained with (13) and (14).

$$t_{on\_SR} = \frac{Q_{GS_{th}} \times R_{G_{ON}}}{V_{drv_{on}} - \left(\frac{V_{GS_{(th)}} + V_{drv_{off}}}{2} \right)} \tag{13}$$

$$t_{off\_SR} = \frac{2Q_{GS_{th}} \times R_{G_{Off}}}{V_{GS_{(th)}} - V_{drv_{off}}} \tag{14}$$

Equation (15) indicates the loss of energy related to the output capacitance (C_{oss}) that occurs on the switch. Direct driving and gate losses are shown at (16) and (17). Direct conduction losses on each transistor should consider the RMS (Root Mean Square) on each switch. Where R_{DS_on} the resistance between Drain and Source, and *D* is the duty cycle.

$$P_{OSS} = 2 f_{sw} \left(\frac{1}{2} \left(C_{oSS_{Q1}} + C_{oSS_{Q2}} \right) V_{sd}^{\ 2} \right) \tag{15}$$

$$P_{cond} = I_D^{\ 2} \times R_{DS_{ON}} \times D \tag{16}$$

$$P_{DRIVING} = V_{drv_{on}} \times Q_G \times fsw \tag{17}$$

III. Simulation and Results

In this section will be presented the results of simulations of the amplifier and the GaN device in the *Psim* software, where results of losses, harmonics and amplitudes were obtained at different frequencies. The GaN Transistor used in the simulations is the TPH2112PS model of the company *Transphorm*. The simulation method in the Psim environment is performed by creating a Data Base device using the transistor data sheet and applying to the thermal module to obtain losses in the GaN component. The simulation is performed using the Psim TI F28335 module from Texas Instruments in which it uses two DAC inputs (Digital Analog Converter), one for the analog signal input and the other for the error signal coming from the voltage sensor at the exit of the amplifier. In each DAC are also used ZOH blocks (Zero Order Retention), a block of differences, a block of the transfer function in the Z domain and the PWM generator blocks, this being a simple and a counter phase. The sampling rate in each of these blocks is twice the switching frequency thus maintaining the *Nyquist* sampling rate. The circuit's schematic is shown in Fig. 6 and 7.

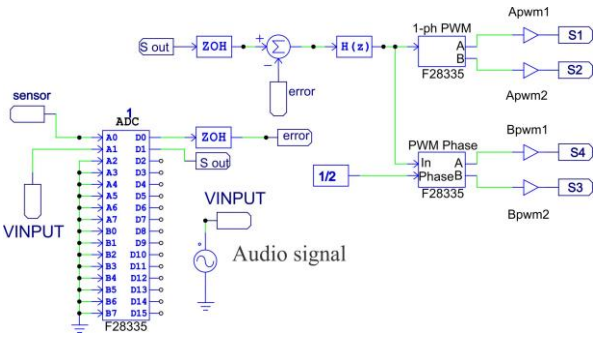

Fig. 6 Blocks used in the *Psim* Simulation.

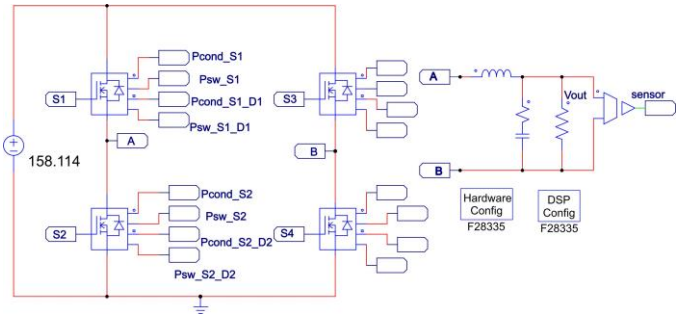

Fig. 7 Output blocks used in *Psim* Simulation.

The paramenters in Table I are applied to the class D amplifier.

TABLE I
DESING PARAMETERS

Amplitude Modulation m_a	0.8
Frequency Modulation m_f	21.053
ΔIL(Current Ripple in the Inductor)	1.098 A
Output Inductor	45.016×10^{-6} H
Output Capacitor	$351{,}686 \times 10^{-9}$F
ΔVC(Voltage Ripple in Output Capacitor)	0.894 V
ESR (Equivalent Series Resistance)	814.75×10^{-3} Ω
Load Resistance	8 Ω
Maximum Audio Signal in dBu and Rms	0 dBu = 0.775 VRms
LC Filter Cut-Off Frequency	40 KHz
DAC Gain	1.204
Amplification Gain	37.6 dB

Considering the resistance of the very small inductor with rl = 0, we analyzed Fig. 5 and obtained the plant transfer function presented in (18). Using the bilinear transformation method, which involves mapping the plane S to plane Z over the unit radius circle, we obtain the following expression in (19) in the equation format the differences in which it is applied to the processor.

$$V_{out} = V_{dc} \cdot \frac{V_{control}}{v_{tri}} \cdot \frac{R \cdot (s \cdot C \cdot E_{SR} + 1)}{R + (L + C \cdot R \cdot E_{SR}) \cdot s + (s \cdot R + E_{SR}) \cdot C \cdot L \cdot s^2} \tag{18}$$

$$y(n) = 8.389y(n-1) - 21.57y(n-2) + 1.058y(n-3) - 8.628y(n-4)$$
$$-0.014u(n) + 1.55u(n-1) - 4.168u(n-2) + 2.836u(n-3) \tag{19}$$

In Fig. 8 we have the waveforms of the output voltage, output current, amplifier input voltage at the frequency of 1KHz and the output voltage of the sensor. This frequency is chosen by convention because it is in a region of great sensitivity to the human ear according to [5].

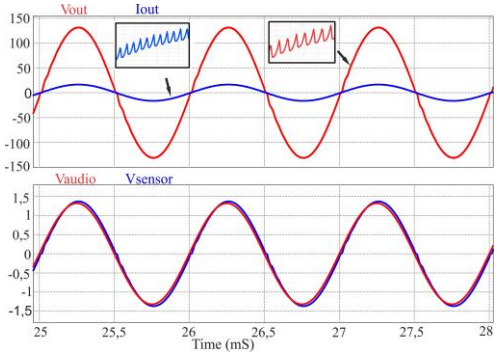

Fig. 8 Voltage waveforms and output current and input voltage and sensor.

Fig. 9 presents an audio signal simulation in order to obtain a waveform that is operating closer to the actual one. In it we have the frequencies of 20Hz, 500Hz, 1KHz, 5KHz, 10KHz and 19KHz with amplitudes of 0.2V peak to 1.32V peak.

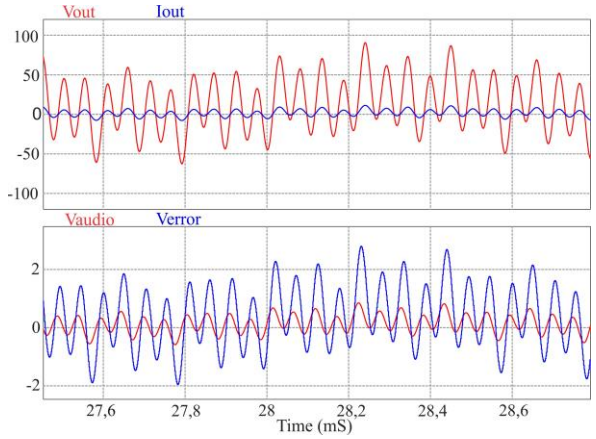

Fig. 9 Audio Signal Simulation.

In the diagram of Fig. 10 we obtain the validation of the transfer function with crossing frequency at 100KHz, a phase margin of 68.899° and infinite gain margin.

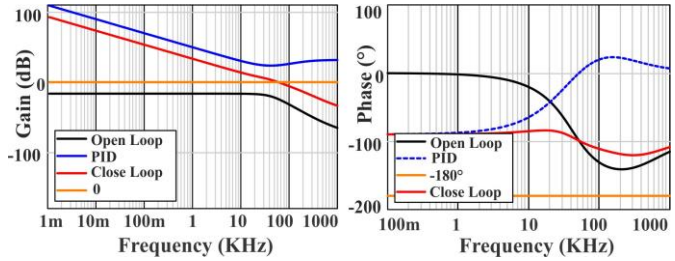

Fig. 10 Transfer Function Diagram.

Fig. 11 presents the validation of the transfer function performed via simulation.

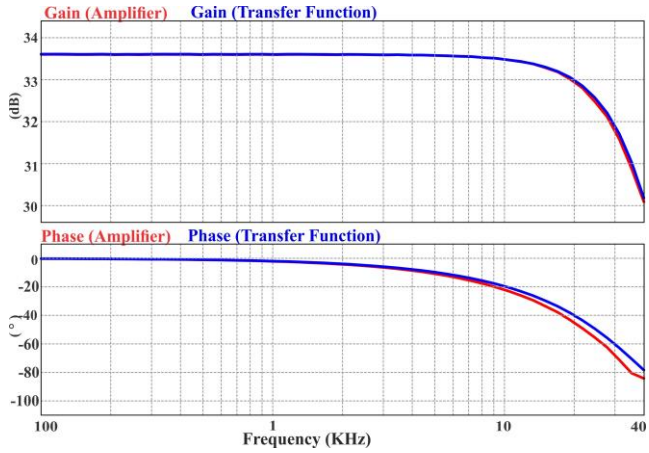

Fig. 11 Simulation of the transfer function to control the output voltage.

In Fig. 12 we have the Fast Fourier Transform (FFT) for harmonics with frequency centered at 1KHz, we have the harmonics located at 2 times the sling frequency and in their multiples.

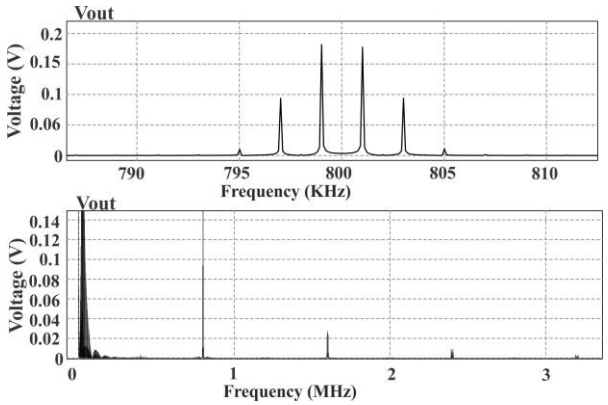

Fig. 12 Harmonics above the slot Frequency.

Table II shows the simulation values presented in Rms values.

TABLE II
SUMULATION RESULT FOR 1 KHz

	Current (A)	Voltage (V)	Power (W)
Input Bus (Vdc)	9,244	111,216	1028,131
Output Load	11,177	89,416	999,410

In Fig. 13 we observed the yield fall in the amplifier at the highest frequencies up to the cutting frequency.

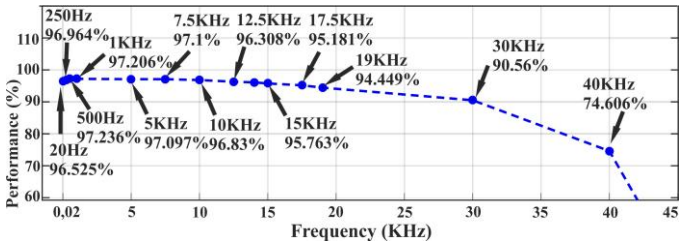

Fig. 13 Yield Curve.

The results of losses due to transistor and yield are presented in Table III.

TABLE III
PERFORMANCE AND LOSS ON AMPLIFIER TO 1 KHz

Efficiency (%)	97.206
THD (%)	0.23
Transistor Losses (W)	1.684
Conduction Losses (W)	6.1089

L. Results of the Prototype

The prototype is developed using the dsPIC33CH Curiosity development board from the company Microchip, in it are used two DAC's in 12 bits and four outputs of PWM in high resolution. This processor was chosen for enabling the main code to be processed at a frequency of 180MHz and the PWM in high resolution at 500MHz, allowing to obtain the 12 bits of audio signal in DAC directly at the signal output in PWM, obtaining a high definition and accuracy in the audio signal. The GaN module, is the Model LMG3411EVM-018 from the company Texas Instruments where it has in each module two GaN's type GaN FET model LMG341Xr050. Fig. 14 presents the physical amplifier, in the tests we obtain in Fig. 15 which is the waveform of output voltage and output current in RMS in

the amplifier for the frequency of 1.012kHz with resistive load of 6.9Ω and in transistors is applied a dead time of 40nS. The voltage is given at 100V per division, and the current at 10A per division. The amplifier yield is shown in Fig. 16 for an RMS power.

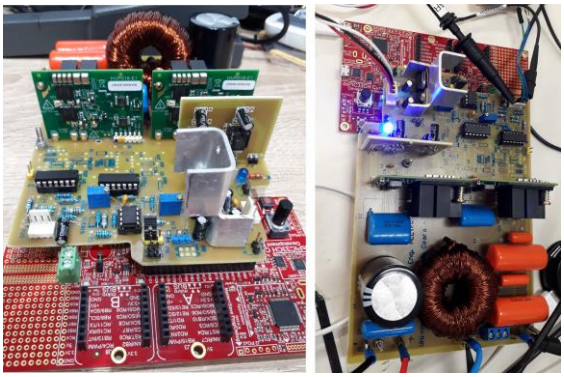

Fig. 14 Prototype.

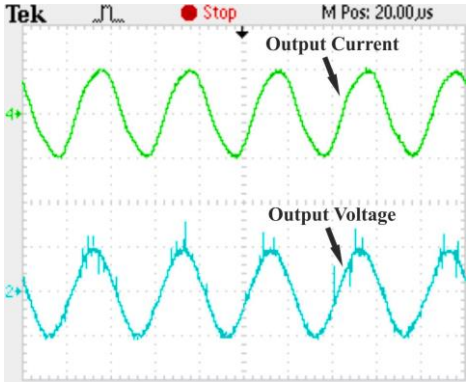

Fig. 15 Voltage and Output Current in the Load.

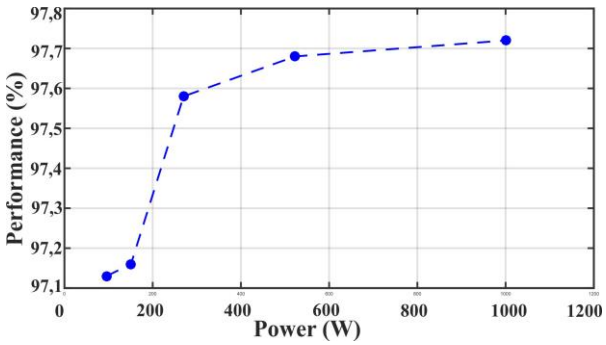

Fig. 16 Yield curve by Power.

IV. CONCLUSION

This work presented the design of digital amplifier with GaN transistors. In it is possible to obtain a yield of 97% in the conversion of audio signal energy to 1KHz per simulation. The losses observed in GaN were only by conduction and switching. The functioning of the control proved to be satisfactory and THD with 0.23% proved to be an acceptable value according to [3] where he points out that this is a critical parameter in class D amplifier, and in [5] he adds that for low-order harmonic frequencies has its notable presences from 1% THD, and distortion values lower than this are little noticeable to the human being. The proposed modulation proves advantages when we analyze the harmonics located well above the cut off frequency of 40 KHz. The performance of the physical amplifier was 97.7% for a maximum power of 1001.04 Watts. In the results with audio, a small low-frequency noise was observed that comes from the power supply and is amplified by the system, showing the need for more filters in the signal input.

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