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***Abstract*—This letter presents a high-performance wide-band divide-by-2 injection-locked frequency divider (ILFD) in the 0.18 µm CMOS process. The ILFD uses transformer-coupled resonator with two resonant frequencies based on the lumped inductor model, and it consists of two sub-ILFDs coupled by inductive coupling. The ILFD can operate in three modes with overlapped locking ranges. The optimal bias condition yields wide locking range at low power with high figure of merit. At the power consumption of 1.83 mW and at the input power of 0 dBm, the locking range is 3.3 GHz from 2.3 to 5.6 GHz. The ILFD can have two non-overlapped locking ranges or an overlapped locking range, this indicates the ILFD uses a dual-resonance resonator.**

Keywords-Dual-resonance transformer-coupled resonator, divide-by-2 injection-locked frequency divider, overlapped locking range.

I. INTRODUCTION

A low-modulus *LC*-tank ILFD is the most important LC-ILFDs and is widely used in phase-locked loops (PLLs) and RF circuits for frequency signal processing. Divide-by-2 transformer-based ILFDs [1]-[4] are one of low-modulus ILFDs. Transformer-based resonator is a dual-resonance resonator with two resonance frequencies at ω_1 and ω_2, the transformer-based ILFD [1]-[3] has two non-overlapped locking ranges around the frequencies $2\omega_1$ and $2\omega_2$. A lot of previous ÷2 ILFDs [4]-[11] using coupled dual-tanks do not show explicitly the advantage of dual-resonance resonator by coupled inductors, because they do not show the phenomena of over-lapped locking ranges. In [10] dual-resonance impedance is simulated, however, the experimental data does not match the simulated results in frequency range. In [11] two locking ranges of transformer-coupled resonator ILFD have not been used explicitly. The ILFD [4] employs the frequency tuning to extend the operation range.

This letter presents a transformer-based ILFD, which has two overlapped locking ranges and it fully utilizes the overlapped locking ranges to emulate a single-band like locking range at a fixed bias. No varactor is used and operation is simple. In general, at low injection power level, locking range increases with injection power, therefore decreasing the supply voltage will reduce the injection power and locking range of ILFD in an integrated system. This indicates that wide locking range ILFD can operate at lower supply voltage with robustness to process, temperature and voltage variation. Dual (triple)-resonance resonators can be implemented in many ways, the right-handed transmission line like resonator [12]-[14] has many inductors to occupy large die area. The transformer-based ILFD can save die area.

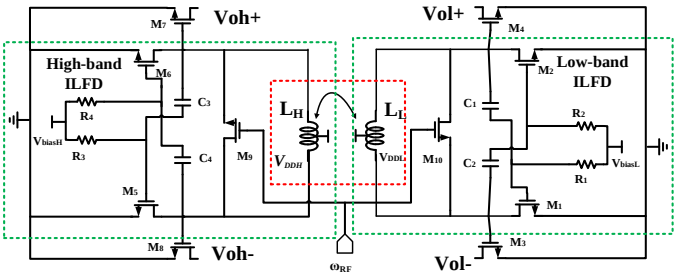


Fig. 1. Schematic of the studied ÷2 ILFD.

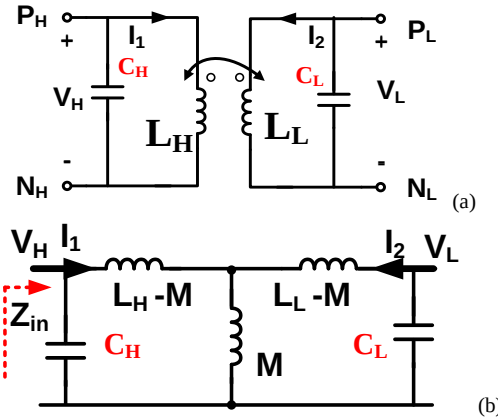


Fig. 2 (a) Schematic of transformer-coupled resonator. (b) Equivalent model of transformer-coupled resonator.

II. CIRCUIT DESIGN

Fig. 1 depicts the schematic of the designed ÷2 ILFD composed of two sub-ILFDs coupled by magnetic field. The first low-band sub-ILFD consists of a resonator due to inductor L_L and a parasitic capacitor C_L in shunt with L_L, and a capacitive cross-coupled pair (M_1, M_2) to generate negative resistance to compensate the resistive *LC*-tank loss. (R_1, R_2) are biasing resistors and (C_1, C_2) are dc blocking resistors. V_{biasL} is the gate bias. As V_{biasL} increases, the power consumption increases because of increasing channel

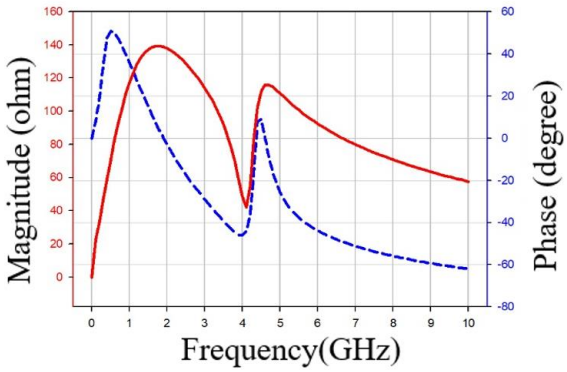


Fig. 3. Simulated input impedance at low-band side.

conductance of (M_1, M_2). The second high-band sub-ILFD consists of a resonator due to inductor L_H and a parasitic capacitor C_H in shunt with L_H, and a capacitive cross-coupled FET pair (M_5, M_6) with (R_3, R_4) biasing resistors and (C_3, C_4) dc blocking resistors. V_{biasH} is the gate bias. The coupled inductors (L_H, L_L) couples the two sub-ILFDs. Transistor M_9 and M_{10} are injection mixers are biased at V_{inj}. (V_{DDH}, V_{DDL}) are supply voltages. (M_3, M_4) and (M_7, M_8) are buffers. The use of capacitive cross-coupled [15] oscillator can tradeoff the power and locking range to obtain better ILFD figure of merit (FOM).

Fig. 2(a) shows the transformer resonator with an equivalent circuit shown in Fig. 2(b), which is a 4th-order LC resonator with two resonant frequencies. The ILFD can operate in three modes with overlapped locking ranges: First ILFD is on and second ILFD is on; first ILFD is on and second ILFD is off; and first ILFD is off and the other is on. Fig. 3 shows the simulated magnitude and phase of the input impedance seen from the low-band side, the resonator has two peak impedance and provides resonant frequencies at 2 GHz and 4.4 GHz.

III. MEASUREMENT

The *LC* tank ÷2 ILFD has been designed and fabricated in the TSMC 0.18 μm CMOS technology. The die micrograph is shown in Fig. 4. The total area including the output buffer and the pads is 0.906 ×0.896 mm^2. The transformer is implemented using concentrically wound octagonal planar spirals.

We first study the case with only either low-band active core on or high-band active core on. Fig. 5 shows the measured input sensitivity for the ÷2 ILFD biased at (a) V_{DDL}=0.6V=V_{DDH}, V_{biasL}= 0.8V,V_{inj}=1.1V, V_{biasH}= 0.0V, and (b) V_{DDL}=0.6V=V_{DDH}, V_{biasH}= 0.8V,V_{inj}=1.1V, V_{biasL}= 0.0V. For the bias condition (a), the low-band free-running oscillation frequency is 1.7 GHz, and at P_{inj}=0 dBm the locking range is 5.9 GHz from 1.6 GHz to 7.5 GHz. At P_{inj}=6 dBm two non-overlapped locking ranges are measured. The conversion gain of mixer related to the transconductance of MOSFET [16] is a function of gate- source overdrive. At low P_{inj} the conversion gain increases with P_{inj} and at high P_{inj} the conversion gain decreases with P_{inj}. This indicates that the locking range at P_{inj}=0 dBm is

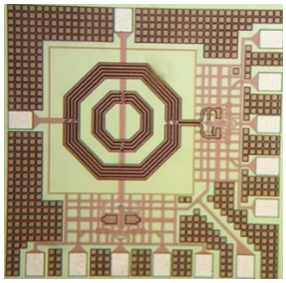


Fig. 4. Chip micrograph for the ÷2 ILFD.

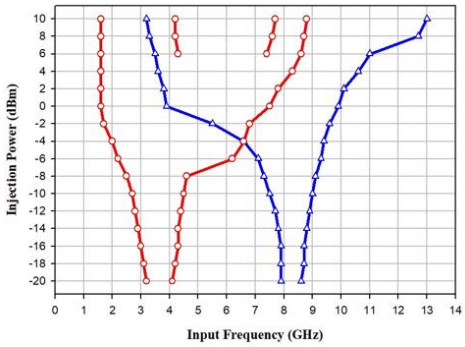
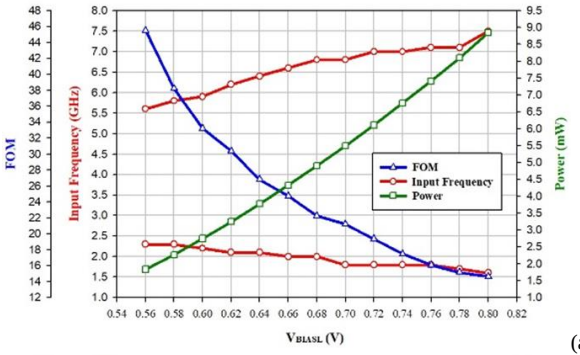
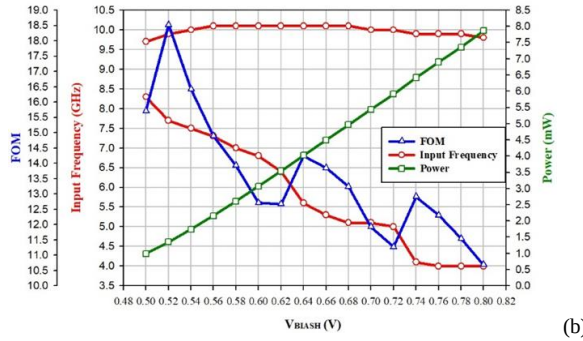


Fig. 5. Input sensitivity plot. (a) Low-band in red color. V_{DDL}=0.6V=V_{DDH}, V_{biasL}= 0.8V,V_{inj}=1.1V.V_{buffer}= 1.0V. V_{biasH}= 0.0V. (b) High-band in blue color. V_{DDL}=0.6V=V_{DDH}, V_{biasH}= 0.8V,V_{inj}=1.1V. V_{biasL}= 0.0V.



(a)



(b)

Fig. 6. (a) Measured locking range at P_{inj}=0 dBm, FOM and power consumption vs V_{biasL}. V_{DDL}=0.6V=V_{DDH}, V_{inj}=1.1V, V_{biasH}= 0 V. V_{biasL}= 0.56~0.8V. Measured at low-band buffer. (b) Measured data vs V_{biasH}. V_{DDL}=0.6V=V_{DDH}, V_{inj}=1.1V. V_{biasL}= 0.0V. V_{biasH}= 0.5~0.8V. Measured at high-band buffer.

overlapped and the non-overlapped locking ranges is due to shrinkage of two locking ranges. For the bias condition (b), the free-running oscillation frequency is 4.1 GHz and at P_{inj}=0 dBm the locking range is 6 GHz from 4 GHz to 10

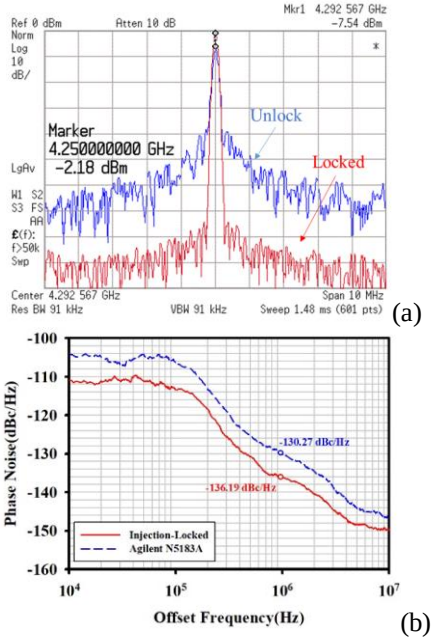


Fig. 7. (a) Measured spectra of the free-running and locked ILFD. (b) Measured phase noises of the RF reference and locked ILFD. V_{DDL}=0.6V=V_{DDH}, V_{inj}=1.1V. V_{biasH}=V_{biasL}= 0.8V. Measured at high-band buffer. f_{inj}=8.5 GHz and P_{inj}=0 dBm.

GHz. The locking range at P_{inj}=6 dBm extends to the the low-band locking range, no visual split locking range is measured. This figure shows the ILFD uses one transformer-based resonator with two resonant frequencies around 1.7 GHz and 4.1 GHz. Fig. 6(a) illustrates the locking range, Figure of merit (FOM) and power consumption versus V_{biasL}. At V_{biasL}= 0.56 V, the power consumption is 1.83 mW, the locking range is 3.3 GHz from 2.3 to 5.6 GHz, the FOM is 46. Figure of merit is equal to Locking Range Percentage/Power Consumption in mW. Fig. 6(b) illustrates the locking range, FOM and power consumption versus V_{biasH}. The high-band peak FOM is lower than the low-band peak FOM. This indicates that the low-band buffer method is a better way of design. The power decreases with decreasing V_{biasH} and V_{biasL} because of lower condutance. Higher FOM is measured at V_{DDL}=0.6V=V_{DDH} > V_{biasL}, V_{biasH}.

Fig. 7(a) superposes the measured spectra of the free-running ILFD and the injection-locked ILFD. The side-band power is larger for the free-running circuit. Fig. 7(b) superposes the two measured phase noises for the input reference and the locked ILFD. The latter has lower phase noise than the former by 5.98 dBc/Hz at 1MHZ offset frequency, this is close to the theory of ideal ILFD.

IV. Conclusion

In this letter a divide-by-2 ILFD is designed in 0.18 μm CMOS process. The ILFD uses two sub-ILFDs share the mutual magnetic field coupling. The ILFD can operate in three operation modes to aid the analysis of the circuit operation. For the one active core is on, the ILFD shows better FOM while it is measured at low-band buffer. In the concurrent oscillation mode, the free-running ILFD outputs two signals at different frequencies. At high injection power, the ILFD shows wide locking range FOM while it is measured at low-band buffer. The ILFD has two oscillation frequencies separated by a frequency gap about 2.4 GHz, which increases the net locking range via the band overlapping.

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