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***Abstract*—A new innovative approach is presented for an efficient and low-power data comparator using multiplexer logic. The proposed method involves the use of a multiplexer-based configuration of the borrow equation within a full subtractor, serving as a fundamental processing element of the data comparator. This model was executed using the Cadence tools and implemented in Verilog for simulation, enhancing its practicality and applicability across different technologies. By integrating a modified borrow equation into the full subtractor design using multiplexers, a decrease in the number of transistors was achieved, resulting in reduced power consumption. Furthermore, a comparative analysis across various technologies revealed substantial reductions in power usage and physical space requirements when transitioning from 180nm to 90nm and 45nm technologies. These findings highlight the potential for considerable power and area savings in practical image processing applications through this innovative approach.**

Keywords—Power Efficiency, Area Optimization,Data Comparator, Full Subtractor, Half Subtractor, 2:1 Multiplexer.

I. INTRODUCTION

A multiplexer-based data comparator is a specialized electronic component designed to efficiently compare digital data inputs using multiplexer circuits, half subtractor, and full subtractors. This design minimizes power dissipation and overall power consumption while reducing hardware complexity compared to traditional comparator architectures. It achieves an optimal balance between energy efficiency and performance, making it suitable for space-constrained applications where optimizing physical space is crucial for efficient system integration and overall performance. Our research aims to reduce the number of transistors in the full subtractor by using this creative design that uses multiplexers. This will ultimately lead to a reduction in power consumption. This work is implemented using Cadence tools, and the suggested design is realized in Verilog for simulation. This focus on usefulness and wide application highlights our dedication to investigating the viability and efficacy of the suggested design in many technological contexts.

The architecture primarily serves image denoising by focusing on minimizing the number of comparators necessary for the sorting process, which is essential for ordering by rank in image processing, organizing pixel values according to their magnitudes [1],[2].

When compared to various logics such as full subtractor(FS) logic and full subtractor multiplexer(FS Mux) logic, the multiplexer based data comparator prioritizes power efficiency in its design approach [3],[4]. The reversible binary comparator evaluates the relationship between two n-bit numbers using a binary tree structure and novel Toffoli Reversible(TR) gate technology. It provides outputs indicating the comparison results of the input numbers [6]. When designing an efficient reversible binary comparator, employing PG gates, CNOT, and NOT, emphasizes optimization in constant inputs, delay, quantum cost, and garbage outputs. This binary comparator design is showcased across varying bit sizes, including 8-bit, 16-bit, 32-bit, and 64-bit numbers [7]. Early design targeting for significant power savings across design levels and utilizing a 4-bit magnitude comparator and BDD driven optimization achieves notable power reduction [8].

Addressing image corruption caused by impulse noise is crucial in image processing and transmission, in VLSI implementation of the Adaptive Rank Order Filter is designed to effectively remove impulse noise [9]. An efficient VLSI hardware implementation for sorting networks, incorporating a novel carry select comparator design for median calculation within 7 clock cycles. Additionally, it presents a novel FSM based architecture for high-density salt and pepper noise removal in images, with the first output appearing after 16 clock cycles in sequential operation [11],[12]. The design of a high-speed, low-power comparator for Analog to Digital Converters in Digital Wireless Communication by utilizing a two-stage CMOS Operational Amplifier circuit with 0.18µm technology, the comparator achieves low power consumption and fast propagation delay [13]. Evaluates various design methodologies for a Logic circuit of 1-bit Magnitude

Comparator, contrasting Gate Diffusion Input Logic, Conventional CMOS, and Pass-Transistor Logic (PTL). GDI Logic demonstrates superior performance, with reduced area utilization, power consumption [14]. Utilizing DSCH for gate-level designs and Microwind for layout generation, this novel approach results in reduced transistor count and lower power consumption for an 8-bit comparator implemented in 90nm technology [15].

An overview of the contributions made by the paper is as follows:

- Designing an 8-bit data comparator utilizing a 2:1 multiplexer as the fundamental building block.
- Technological Advancements in Area and Power Efficiency: The transition from 180nm to 90nm and 45nm technologies demonstrates significant reductions in both area and power consumption

To achieve all objectives, the process involves sequential steps beginning with schematic entry, followed by simulation, layout design, physical verification, RC extraction, and concluding with generating Graphical Data System(GDS) files. This comprehensive approach ensures thorough validation and optimization at each stage, facilitating the development of efficient and reliable integrated circuits.

II. PROPOSED ARCHITECTURE

The one extremely helpful combinational circuit for comparing or evaluating two binary numbers is the comparator. A fundamental comparator's key component is an XOR gate, a logic gate with two inputs and one output. The XOR gate produces a high output (logic 1) only when the inputs differ, and it yields a low output (logic 0) when the inputs are the same. This property is key to the comparator's operation. By cascading multiple XOR gates, a comparator can evaluate entire binary numbers bit by bit, determining whether one number is greater than, less than, or equal to another. This comparison process is crucial in various digital systems, such as arithmetic units, data-sorting algorithms, and decision-making circuits.

In the domain of comparators, two fundamental types stand out the Identity Comparator and the Comparator of Magnitude. The Identity Comparator serves to discern the equality of two inputs, whereas the Comparator of Magnitude extends its functionality beyond mere equality determination. Instead of using XOR gates, a multiplexer-based comparator, a 2:1 multiplexer logic is utilized to demonstrate comparator logic. this method can provide flexibility and efficiency in certain comparator designs, catering to specific application requirements within digital systems.

A. Half Subtractor

A half subtractor is a crucial combinational circuit utilized for subtracting one binary digit (bit) from another. In the comparator model half subtractor is specifically designed to facilitate borrow generation, the half subtractor operates with two single-bit inputs, denoted as 'X' and 'Y'.

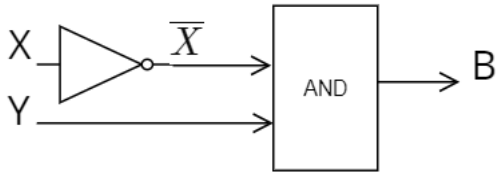

Fig. 1. Half Subtractor

Boolean equation for the Half Subtractor **B=X'Y**(1)

TABLE I. TRUTH TABLE FOR AN HALF SUBTRACTOR OUTPUT AS BORROW B

X	Y	B
0	0	0
0	1	1
1	0	0
1	1	0

B. Full Subtractor

A full subtractor is used for subtracting three input bits the minuend (X), the subtrahend (Y), and the borrow from the previous lower significant bit (Z). It consists of three primary logic gates: an AND gate, an OR gate, and a 2:1 multiplexer. Inputs 'Y' and 'Z' are directed to both the AND and OR gates. The outputs of these gates are then connected to the inputs of a 2:1 multiplexer, where the OR gate output is linked to the 0 input and the AND gate output to the 1 input.

In a full subtractor, the borrow from the previous lower significant bit (Z) is taken into account during subtraction. Therefore, the selection line for the multiplexer, denoted as 'X', determines whether the borrow input is considered in the subtraction process. The final output of the multiplexer represents the output of the full subtractor, providing the difference between the minuend and subtrahend along with the borrow output.

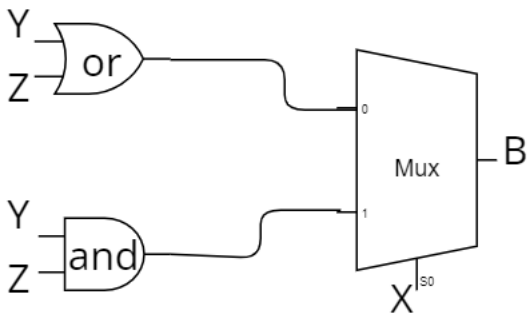

Fig. 2. Full Subtractor

Boolean equation for the Full Subtractor:

Bout=(X'(Y+Z))+(X(YZ)) (2)

TABLE II. TRUTH TABLE FOR THE FULL SUBTRACTOR, OUTPUT AS BORROW B

X	Y	Z	B
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

C. Borrow Propagation Block

The borrow generating unit processes two 8-bit inputs, X[0:7] and Y[0:7]. The least significant bits of these inputs are directed to the first half subtractor, while the remaining bits feed into seven full subtractors. Each full subtractor's borrow output is chained to the next full subtractor's borrow input, forming a continuous cascade. The final borrow output from the seventh full subtractor serves as the ultimate borrow for this unit. This output directly controls the selection line of muliplexer chain 1(Eight 2:1 multiplexers are utilized, each operating with the same selection line as output of borrow generating unit), while its complement is directed to the selection line of multiplexer chain 2.

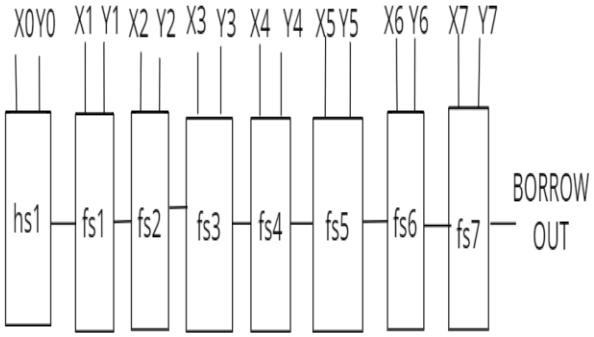

Fig. 3. Borrow Generation unit

$$\textbf{Bout= Z(XY+X'Y')+X'Y(Z+Z')}, \quad (3)$$

$$\textbf{Bout= X'Y'Z+X'YZ'+X'YZ+XYZ} \quad (4)$$

here ‘X’,’Y’ are inputs, ‘Z’ is Input borrow and ‘Bout’ is Output borrow

D. High-Low Selector Multiplexer

After the borrow generating unit generates either '1' or '0', this single bit serves as the selection line for two chains of 8-2:1 multiplexers.One chain receives the borrow output directly, while the other receives its complement. Inputs A[7:0] and B[7:0] are sequentially fed into each mux. The output of the first chain of multiplexers selects the higher value from A and B, while the output of the second chain selects the lower value.

When the input values are A[7:0]=64 and B[7:0]=80, the first output indicates the higher value, 80, while the second output corresponds to the lower value, 64. This comparison process exemplifies the functionality of the comparator, effectively determining the relative magnitudes of the input numbers

TABLE III. TRUTH TABLE FOR DATA COMPARATOR

A[7:0]	B[7:0]	Out 1 (HIGH)	Out 2 (LOW)
01000000 (64)	01000001 (65)	01000001 (65)	01000000 (64)
00011000 (24)	00101001 (81)	00101001 (81)	00011000 (24)
01000001 (65)	00001100 (12)	01000001 (65)	00001100 (12)

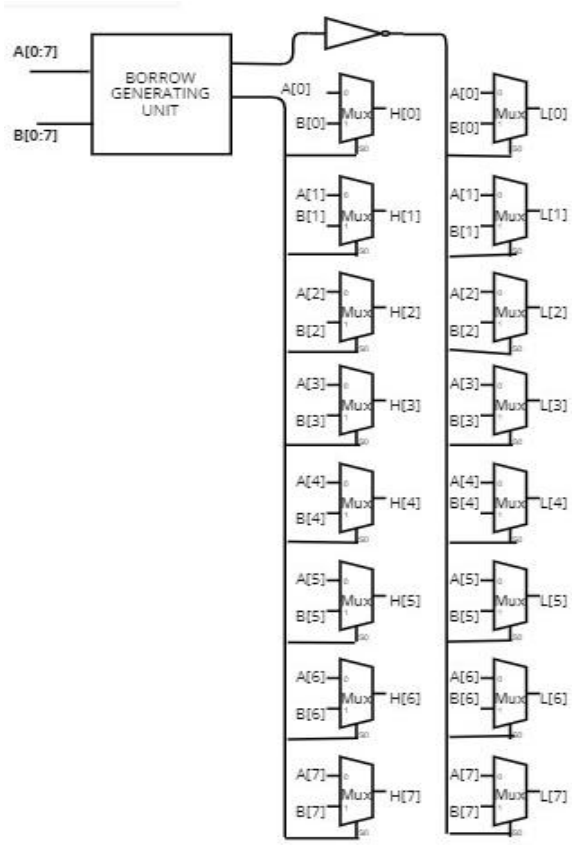

Fig. 4. Multiplexer high and low value output generating unit

III. RESULTS AND COMPARISIONS

After simulating the entire module using the Cadence NCLaunch tool, waveforms are generated by providing various inputs. Subsequently, the module is simulated again in the Cadence Innovus tool to obtain power and area metrics for the comparator across different technologies. Comparison

of these power and area reports led to the generation of the following tables.

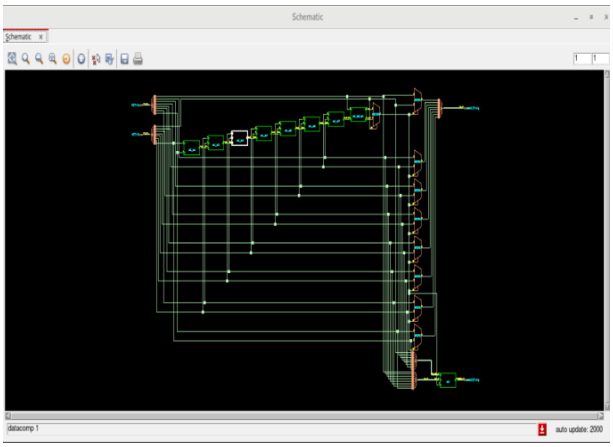

Fig. 5. RTL schematic of 8-bit Data Comparator Using Multiplexer Logic

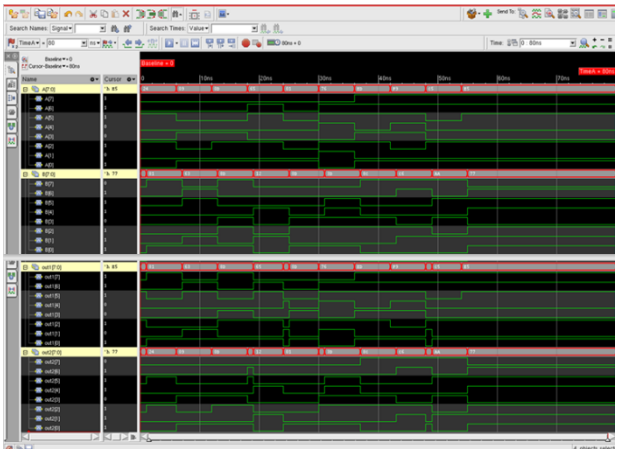

Fig. 6. Simulated results of 8-bit Data Comparator Using Multiplexer Logic

TABLE IV. POWER AND AREA COMPARISON ACROSS THREE TECHNOLOGIES

Technology	Power(mW)	Area(um^2)
45 nm	0.177	63.954
90 nm	0.350	230.8545
180 nm	1.453	814.968

In Table IV, a comprehensive analysis of the power and area for the 8-bit data comparator using multiplexer logic is presented across different semiconductor fabrication technologies, namely 45nm, 90nm, and 180nm. The findings indicate a notable reduction in both power consumption and required area when employing the 45nm technology, compared to 90nm and 180nm technologies.

This reduction underscores the efficiency and optimization achieved in the design of the multiplexer-based data comparator, particularly in the context of varying VLSI technologies.

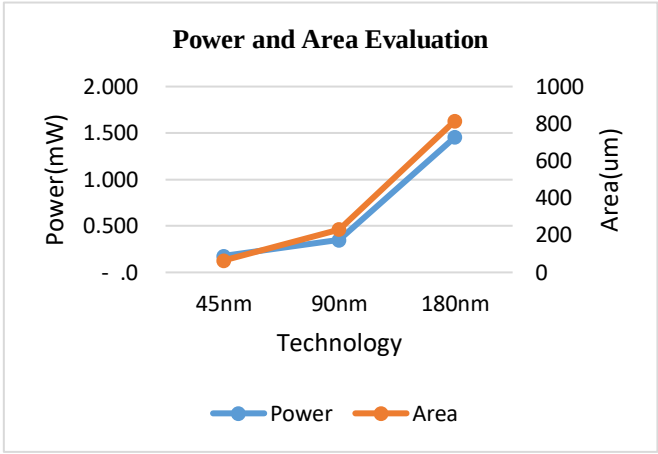

Fig. 7. Comparison Analysis of Power and Area Across Three Technologies

TABLE V. COMPARATIVE ANALYSIS OF DIFFERENT POWER TYPES ACROSS THREE TECHNOLOGIES

Technology	Internal Power(mW)	Switching Power(mW)	Leakage Power(mW)
45nm	0.11974901	0.05727569	0.00000863
90nm	0.24679382	0.10027528	0.00294329
180nm	0.93670402	0.51627163	0.00004000

here **Total Power = Internal Power + Switching Power + Leakage Power.**

Total power consumption is typically broken down into three main components: internal power, switching power, and leakage power. Internal power refers to the energy dissipated within the integrated circuit due to resistive losses and dynamic power consumption during signal transitions.

Switching power accounts for the power consumed during the charging and discharging of capacitive loads as digital signals transition between logic states, primarily influenced by the frequency of these transitions. Leakage power, on the other hand, represents the static power dissipation caused by sub threshold leakage currents flowing through transistors even when they are not actively switching. This component becomes increasingly significant in modern VLSI technologies as transistor sizes shrink, leading to higher leakage currents. By meticulously managing and optimizing each of these power components.

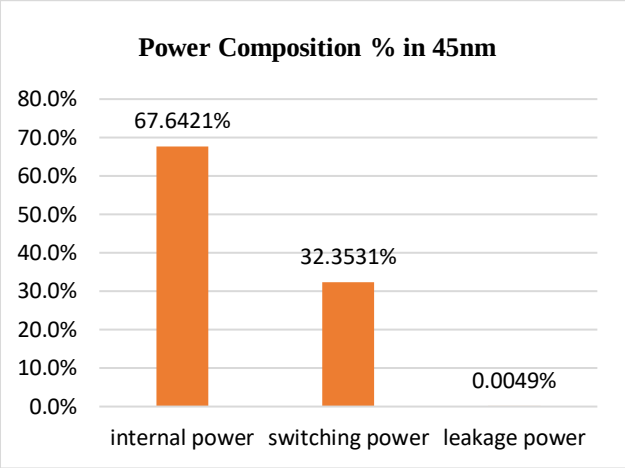

Fig. 8. Comparative Analysis of Internal, Switching, and Leakage Power at 45nm

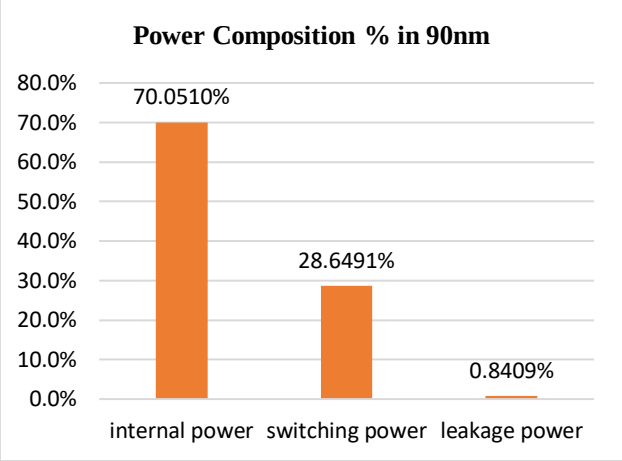

Fig. 9. Comparative Analysis of Internal, Switching, and Leakage Power at 90nm

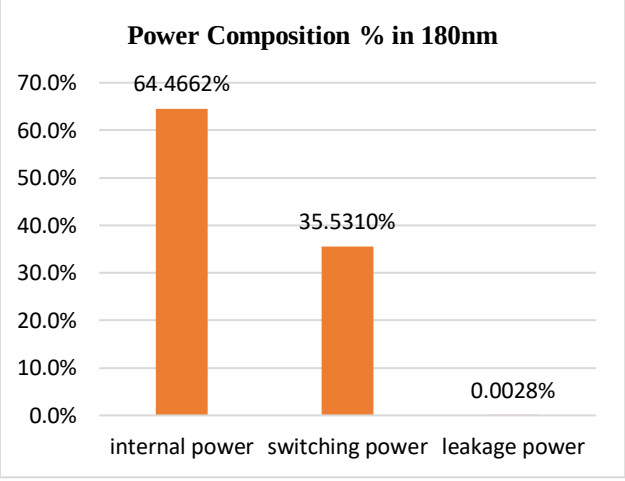

Fig. 10. Comparative Analysis of Internal, Switching, and Leakage Power at 180nm

IV. CONCLUSION

This paper proposes a multiplexer-based data comparator designed for different technologies, including 45nm, 90nm, and 180nm. It focuses on optimizing area and power through the implementation of an 8-bit multiplexer-based data comparator across these technologies using Cadence tools. The reduction in power and area is realized through efficient comparator design and technology migration from 180nm to 45nm. In future research, exploring advanced optimization techniques could lead to even greater reductions in power consumption and area utilization.

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