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A CLASS AB Operational Transconductance Amplifier (OTA) with a Slew-Rate Enhancement (SRE) Auxiliary Circuit

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***Abstract*— This paper introduces a CLASS AB Operational Transconductance Amplifier(OTA) with a slew-rate enhancement (SRE) auxiliary circuit through 0.18um BCD process. The presented OTA is composed of four parts: folded cascode input stage, class AB output stage, SRE auxiliary circuit, reference current source. The proposed OTA achieving the DC gain of 134 dB, unity gain bandwidth of 3.69 MHz under the conditions of 30V power supply voltage and 10pF capacitive load. The simulation results show that the CLASS AB OTA with the proposed SRE auxiliary circuit achieves the positive slew-rate of 140 MV/s and the negative slew-rate of 143 MV/s with a load capacitance of 10pF,which has been increased to a factor of 70 and 89.37 times respectively, while the supply current only increased 7.69%.**

Keywords—Operational Transconductance Amplifier(OTA), CLASS-AB, slew-rate enhancement(SRE) auxiliary circuit.

I. INTRODUCTION

As the most important basic unit in analog integrated circuits, Operational Transconductance Amplifiers(OTA) are used in various circuit systems, such as industrial control, electronic communications and other fields[1]. Among them, digital-to-analog converter(DAC)[2],analog-to-digital converter (ADC)[3], and switched-capacitor(SC)[4]as an essential structural component places the high requirement on the processing speed of the OTA. On the one hand, the slew-rate and bandwidth reflect the speed of OTA. The slew-rate reflects the speed of processing large signal change, while the bandwidth reflects the speed of processing small signal change[5].

In this paper, a CLASS AB OTA with a SRE auxiliary circuit is achieved. The CLASS AB OTA adopt two-stage structure, which the first stage is designed to a folded cascode to meet the requirement of high DC gain, the output stage selects the CLASS AB output structure. Besides, the high slew-rate achieved by two additional currents during a large signal change. The additional currents separately increase the push and pull current of the OTA's first stage to charge the miller capicitors connecting the gate and the souce of the push and pull transistors quickly. Thus the limitation of the slew rate caused by the limited input stage tail current is elimated.

This paper is organized as follows: Section II describes the block diagram of the proposed OTA, the detail circuit implementation and the analysis. Section III introduces the principle of the proposed SRE auxiliary circuit in detail and the OTA's response of the positive and negative large signal change with and without SRE auxiliary circuit. Section IV, the simulation results of the OTA's stability and the comparisons between the CLASS-AB OTA with and without SRE auxiliary circuit are shown. Section V briefly concludes this paper.

II. THE CIRCUIT IMPLENTATION AND THE ANALYSIS OF THE PROPOSED OTA

This part describes the detail circuit implementation and the analysis of the OTA. The Fig.1 shows the block diagram of it. As the Fig.1 shown, the OTA is composed of four modules: folded cascode input stage, SRE auxiliary circuit, CLASS AB output stage, reference current source.

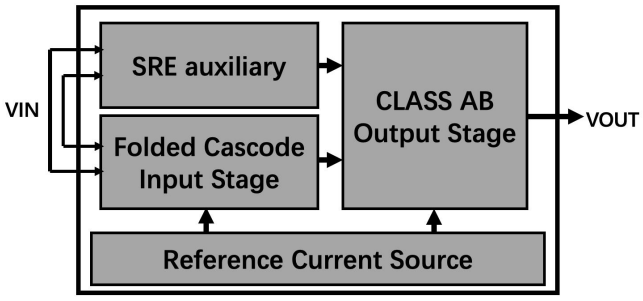


Fig.1 The block diagram of this OTA .

A. Reference Current Source

The Fig.2 shows the schematic of the reference current source. The source is a proportional to absolute temperature(PTAT) current, which is produced by the difference in the voltage of the V_{be}. As shown in the Fig.2, the V_{be} of the T1, T2, T3 and T4 satisfy equation(1):

$$V_{be\,T1}+V_{be\,T4}+I_1R_1=V_{be\,T2}+V_{be\,T3} \tag{1}$$

When the bipolar work in the amplification region, the current of the collect and the V_{be} satisfy equation(2) :

$$I_C = I_{SS} e^{V_{be}/V_T} \tag{2}$$

Conbining the equation(1) and (2), the current I1 of the R1 satisfy equation(3)[6],which the N is the scale factor of the Bipolar's area :

$$I_1 = \frac{2V_T \ln(N)}{R_1} \tag{3}$$

The VBIAS1,VBIAS2, VBIAS3 and the VBIAS4 bias the voltage of the gate of the transistors in the OTA. Through the current mirror, the OTA get the reference current source I1 by the scale factor of the transistors'size,W/L.

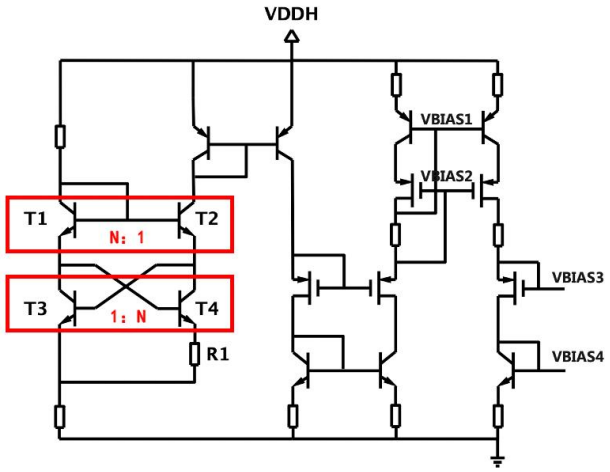


Fig.2. The schematic of reference current source.

B. *Folded Cascode Input Stage And The CLASS AB Output Stage*

The Fig. 3 shows the circuit of a CLASS AB OTA. The first stage is folded cascode structure of PMOS input pairs, which achieving the high DC gain and large input voltage swing simultaneously.

The output stage of the OTA is a CLASS AB push-pull structure. The quiescent current of the push and pull transistors M4 and M8 is controlled by two translinear loop. The M4 in the loop1 consisting of M1, M2, M3 and M4, and the M8 is in the loop2 consisting of M5, M6, M7 and M8. Under conditions of normal and large signal change, any transistors in two translinear loops work in strong inversion. MOS translinear loop circuit principle in strong inversion derived in [7] is shown in (4), Where V_{th} is the threshold voltage, β is the coefficient of device, CW and CCW refer to the connected directions of the devices, clockwise and counterclockwise respectively. For simplicity, the V_{th} of the NMOS and PMOS is designed to be equal respectively. The current equation of the loop1 and loop2 described by (5) and (6) respectively:

$$\sum CW\left(V_{th} + \sqrt{I_d/\beta}\right) = \sum CCW\left(V_{th} + \sqrt{I_d/\beta}\right) \tag{4}$$

$$\sqrt{\frac{I_{M1}}{\left(\frac{W}{L}\right)_{M1}}} + \sqrt{\frac{I_{M2}}{\left(\frac{W}{L}\right)_{M2}}} = \sqrt{\frac{I_{M3}}{\left(\frac{W}{L}\right)_{M3}}} + \sqrt{\frac{I_{M4}}{\left(\frac{W}{L}\right)_{M4}}} \tag{5}$$

$$\sqrt{\frac{I_{M5}}{\left(\frac{W}{L}\right)_{M5}}} + \sqrt{\frac{I_{M6}}{\left(\frac{W}{L}\right)_{M6}}} = \sqrt{\frac{I_{M7}}{\left(\frac{W}{L}\right)_{M7}}} + \sqrt{\frac{I_{M8}}{\left(\frac{W}{L}\right)_{M8}}} \tag{6}$$

It can be derived from (5) and (6) that the current of the other three transistors in loop1 and loop2 is ensured. The static current of the push and pull transistor, M4 and M8, is ensured.

III. The Detail Circuit Of The SRE Auxiliary And The Operation Of The OTA With and Without SRE Circuit

A. *The SRE Detail Circuit*

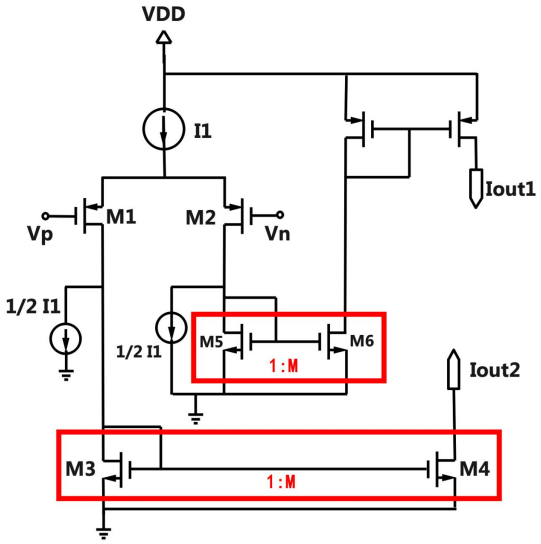


Fig.4. The detail circuit of the SRE auxiliary.

Fig.4 shows the proposed SRE auxiliary circuit. Under small signal change conditions, the differential input transistors M1 and M2 have same current dividing the tail current provided by the current source I1. At this time, the transistor M1 and transistor M2 have almost no current. The current of the M3 and M4 is M times larger than the current of M1 and M2, through designing the W/L of the transistors with factor M. Thus, under no and small signal change condition, the SRE auxiliary circuit is off and have no current to output, Iout1=Iout2=0. When the large signal change is positive, the voltage of M1's gate suddenly increased significantly. Almost all of the tail current I1 flows through the branch of the transistor M1. Offseting the current 1/2I1 , the current of the M2 is increased to 1/2I1. By the factor M of the current mirror, the output current Iout1=M/2I1,while the Iout2=0. In the same manner, when the large signal change is negative, the output current

Iout2=M/2I1, while Iout1=0. Generally speaking, the SRE auxiliary circuit will separately supply an additional current during positive and negative large signal change. In this paper, The factor M is designed samely to ensure symmetric slew-rate enhancement for the CLASS-AB OTA.

B. *The Operational Of The OTA Without SRE auxiliary circuit*

In Fig.5, the input and output voltage, most current derection are marked by diffderent color. When the large signal change is positive， as the red color marked acting, almost all of the tail current of the input stage flows through the right input transistor, almost none current flows through the left. Because the current produced by the bias voltage VBIAS3 and VBIAS4 is unchanged ,so the current of the M3's source and M7's drain is larger than the M3's drain and M7's source, so the difference in current charges the millor capicator to increase the output voltage. When the tail current of the input stage is 2 times larger than the current produced by VBIAS3 and VBIAS4, the slew-rate of the OTA is decided by the tail current of the input stage and the miller capicator, shown in equation(7), SR is the slew-rate of the OTA, I_{tail} is the tail current of the OTA's input stage, C_{miller} is the compensation capicator.

$$SR = \frac{I_{tail}}{C_{miller}} \tag{7}$$

In the same manner, when the large signal change is negative, as the blue color marked acting, almost all of the tail current of the input stage flows through the left input transistor instead of the right, while almost none current flows through the left, so the current of the M3's source and M7's drain is smaller than the M3's drain and M7's source, so the difference in current discharges the millor capicator to decrease the output voltage. The formula of the OTA's slew-rate is same as formula(7).

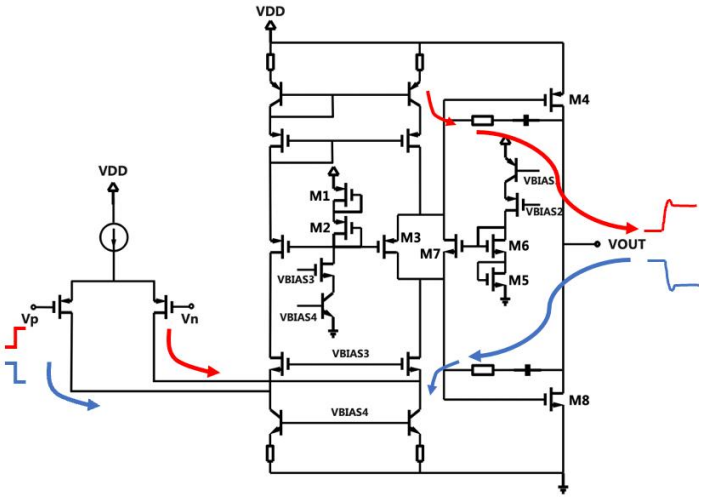


Fig.5 The current condition of the OTA without SRE auxiliary circuit.

C. *The Operational Of The OTA With SRE auxiliary circuit*

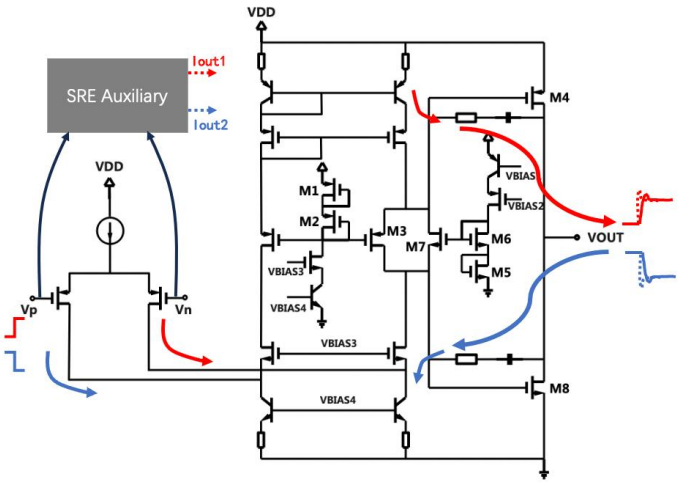


Fig.6 The current condition of the OTA with SRE auxiliary circuit.

As the Fig.6 shown, with the designed SRE auxiliary circuit, the charging and the discharging current is increased by the Iout1 and Iout2, which decided by the tail current of the SRE auciliary circuit and the scale factor M of the transistors, then the equation(7) became the equation(8):

$$SR = \frac{I_{tail} + M/2I_1}{C_{miller}} \tag{8}$$

It can be concluded from the equation(8) that the slew rate is increased by the SRE auxiliary circuit. The more M is, the larger slew-rate of the OTA is.

IV. Simulation Result

The design and the simulation is worked by Cadance® Spectre®. The Fig.7 shows the simulation result of the OTA's stability with the 10pF capicator load.

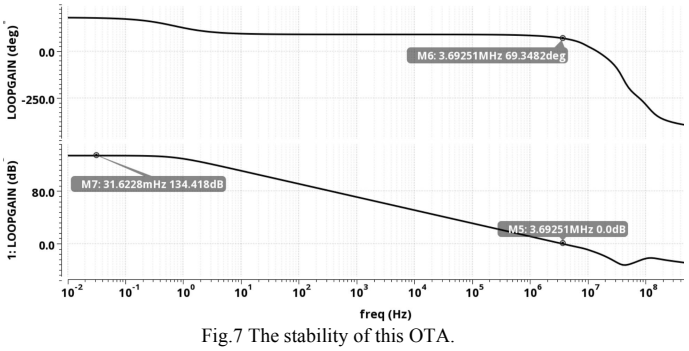


Fig.7 The stability of this OTA.

It can be derived that the bandwidth of the OTA is 3.69MHz.

The Fig.8 and Fig.9 show the simulation results of the OTA with and without SRE auxiliary circuit with input voltage is given a rising step voltage from 0V to 2.5V and a falling step voltage from 2.5V to 0V.

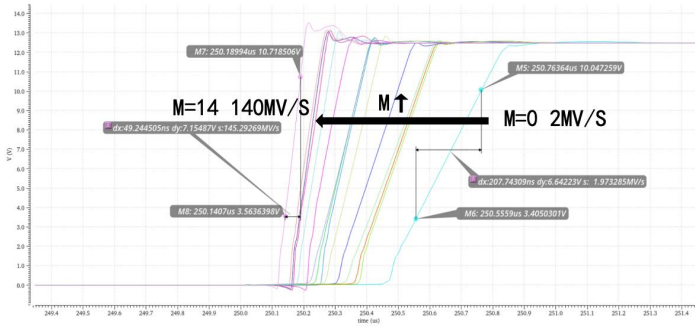


Fig.8. The simulation result of positive step responses.

The rising step response of the OTA's output voltage with and without SRE auxiliary circuit are shown in Fig.8. The slew rate of CLASS AB amplifier with SRE auxiliary circuit,M>0, has been improved than its of OTA without SRE auxiliary circuit,M=0. With the greater the increase in M,the greater the slew-rate of the OTA, when M=14, the slew -rate of the OTA is 140 MV/s, which is larger 70 times than it of M=0.

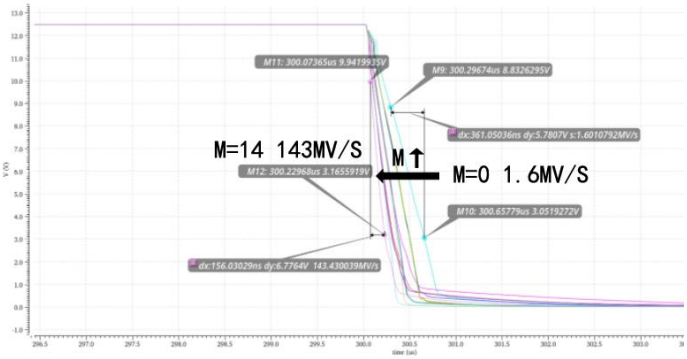


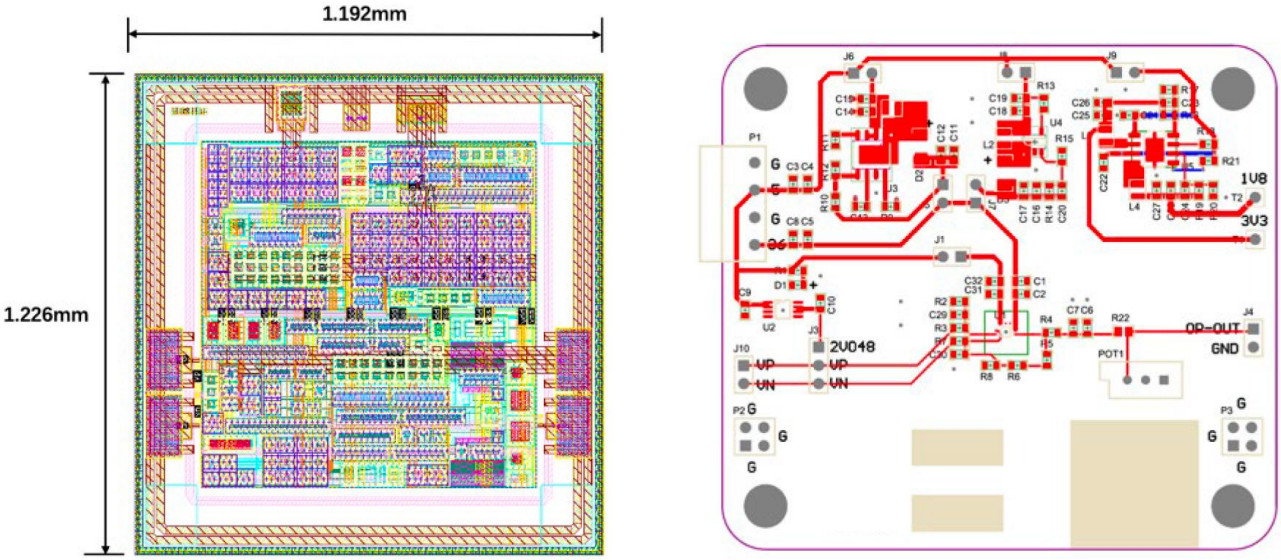
Fig.9 The simulation result of negative step responses.

The falling step response of the OTA's output voltage are shown in Fig.9. Performed samely as the positive response, with the greater the increase in M,the greater the slew-rate of the OTA, when M=14, the slew-rate of the OTA is 143 MV/s, which is larger 89.37 times than it of M=0.

The parameters comparisons of the OTA without and with the proposed SRE auxiliary circuit are shown in Table I. It can be referred that the slew rate has significant improvement by the proposed SRE auxiliary circuit. With the scale factor M of the transistors'size increased, the positive and negative of the OTA's slew-rate have been improved more and more. The max positive and negative slew-rate has been improved 70times, 89.37 times respectively with the same scale of the transistors in the SRE auxiliary circuit, M=14, with the high supply voltage of output stage, VDDH=30V and with the same load capacitor of 10pF, while the supply current only increased 7.69%. The Fig.10 shows the layout of the proposed OTA and the test PCB.

V. CONCLUSION

In this paper, a CLASS AB OTA with a SRE auxiliary circuit achieved by two additional current during the large signal change is presented. The OTA have 3.69M Hz bandwidth and maintain the stability with the 10pF capicator load. Even, a SRE auxiliary designed for the OTA. Through adjusting the scale factor M of the transistors in the SRE auxiliary circuit to get the required slew-rate of the OTA. The positive slew-rate has been improved 70 times, negative slew-rate has been improved 89.37 times with the factor M=14, the same supply voltage, same capacitor load with the supply current only increased by a factor of 7.69%, which is proven that the designed SRE auxiliary circuit provides a superior performance in terms of slew rate of the proposed CLASS AB OTA.



(a) (b)

Fig.10 The Layout of the OTA (a) and the test PCB (b).

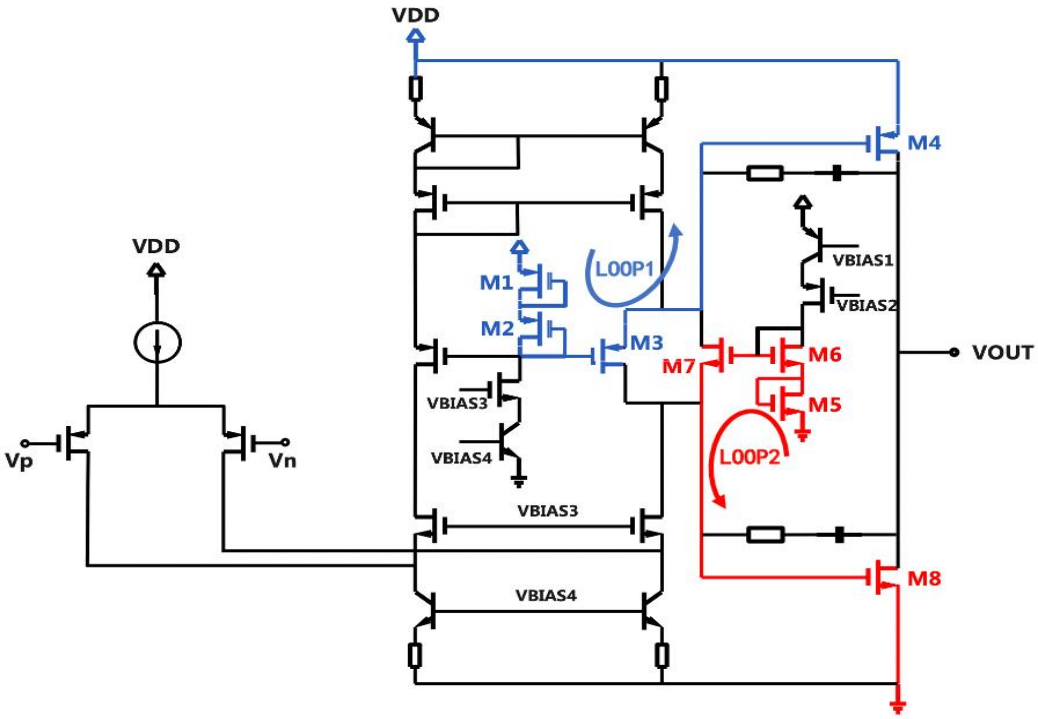


Fig.3 The schematic of the OTA's input stage and CLASS AB output stage.

TABLE I THE CONPAIRASION DATA OF THE OTA WITH AND WITHOUT SRE AUXILIARY CIRCUIT.

	w/o SRE M=0	**w SRE M=4**	**w SRE M=8**	**w SRE M=12**	**w SRE M=14**	**change(MAX)**
supply voltage(V)	30	30	30	30	30	0%
supply current(μA)	130	140	140	140	140	7.69%
output capacitor(pF)	10	10	10	10	10	0%
slew rate positive(MV/s)	2	9.8	40.9	93.2	140	70times
Slew rate Negative(MV/s)	1.6	10.6	57.2	98.6	143	89.37times

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