Kalpa Publications in Engineering
Volume 1, 2017, Pages 187–192
ICRISET2017. International Conference on Research and Innovations in Science, Engineering &Technology. Selected Papers in Engineering

An Overview on Problem of Balancing Of DC Capacitor Voltage in Diode-Clamped Multilevel Inverter Using Boost Converter

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Abstract

Multilevel inverter allows the production of high voltage with lower harmonic distortion in ac output and it eliminates the need of transformer. With the usage of multilevel inverter, we can get the required ac voltage output from multiple dc voltage rails. One of the disadvantage in it is the unbalancing of dc link capacitor voltage. The basic aim of this paper is the balancing of dc link capacitor voltage in diode-clamped multilevel inverter. There are different approaches which could be used for balancing of the capacitor voltage. In this paper, the method of additional auxiliary circuit in the form of Two-level Boost converter is being adopted to balance the inner capacitor voltages so as to get the required multilevel output. This balancing leads to the reliability in the inverter output voltage and extension in life of capacitor. The simulations for this are being performed in MATLAB SIMULINK® and the result are being analyzed for the same by employing it for different load condition. The scheme thus offer the proper balancing of capacitor voltage.

Keywords

DC link Capacitor voltage balancing; diode-clamped multilevel inverter; LC filter; Two-level boost converter

1 Introduction

There are basically three types of highly popular voltage source multilevel inverters. They are being categorized based on their network topologies as diode-clamped multilevel inverter or neutral point clamped inverter, flying capacitor multilevel inverter and cascaded or H-Bridge inverter [1].

A. Shukla, J.M. Patel, P.D. Solanki, K.B. Judal, R.K. Shukla, R.A. Thakkar, N.P. Gajjar, N.J. Kothari, S. Saha, S.K. Joshi, S.R. Joshi, P. Darji, S. Dambhare, B.R. Parekh, P.M. George, A.M. Trivedi, T.D. Pawar, M.B. Shah, V.J. Patel, M.S. Holia, R.P. Mehta, J.M. Rathod, B.C. Goradiya and D.K. Patel (eds.), ICRISET2017 (Kalpa Publications in Engineering, vol. 1), pp. 187–192

This different multilevel inverter could be used in applications like static VAR compensators, variable speed motor drives, high voltage grid interconnection. From the studies carried out earlier it has been found that the method of using passive front end capacitor voltage balancing is only possible if the modulation index is limited to 60% of the inverter load and 0.8 power factor.

This limitation could be overcome by using different techniques such as inverter being supplied by isolated dc sources, using of the balancing circuit that transfers the the additional charge acquired to the uncharged capacitor or the modification of pulse width modulation switching pattern [2].

To avoid the extra cost involved in the additional balancing circuit many authors suggested in modifying the switching pattern,but this method had several of the limitation.PWM strategy once employed alone could not cope up with the problems like total harmonic distortation,Common mode voltage cancellation and leakage current.To avoid this limitation a modified boost converter in the form of Two Level boost converter[TLBC] is being employed.It is advantageous in high voltage applications because of reduced switching losses and reduced recovery losses and the requirement of lower inductor size for providing the additional voltage.Also the current ripple is halved compared to conventional boost converter [3][4].Therefore in this paper dc voltage balancing of inner capacitor is performed using two level boost converter.

2 Diode clamped multilevel inverter

Three level neutral point clamped converter was proposed by Nabae et.al in 1981.In a total there were two capacitors connected in series to form an additional level. It is being named as neutral point clamped inverter because the additional level of this was the neutral point of the dc bus. Diode-clamped multilevel inverter/neutral point clamped inverter is one of the most conventional topology in multilevel inverters where diode is being used to clamp the dc output voltage to obtain the desired output. A single-phase inverter consists of (m-1) dc link capacitors,2(m-1) switching devices and (m-1) (m-2) clamping diodes [1]. This is shown in fig 1.

To get the desired output voltage the switches as shown in fig.1 are turned on accordingly as follows [1]

Here the upper switches are referred to as S_1-S_4 and lower switches as S_1'-S_4'.

1.For voltage level =Vdc/2 all upper switches are turned on.

2.For voltage level =Vdc/4 three upper and one lower switch is turned on.

3.For Voltage level=0 two upper and two lower switches are turned on.

4.For voltage level =-Vdc/4 one upper and three lower switches are turned on

5.For voltage level =-Vdc/2 all lower switches are turned on.

Disadvantage/limitation observed in diode clamped multilevel inverter is the need of additional clamping diodes and dc link capacitor voltage unbalancing.

The total dc voltage is being equally distributed across the dc link of the capacitor but due to the different duration working of the capacitors some of the capacitors used up are more frequent than the other. As shown in fig.2 during a particular interval both capacitors C_1 and C_2 are used. During this time both the capacitors discharges. But after some interval of time again the capacitor C_2 is being used up to supply the load so it keeps on discharging. So, if this voltage is not being balanced it further leads to the condition where the inner capacitors voltage is nearly zero due to this the multilevel inverter start behaving as a simple three level inverter.This voltage unbalancing exists regardless of different load condition [1] for this a strategy of voltage balancing of dc link capacitor.

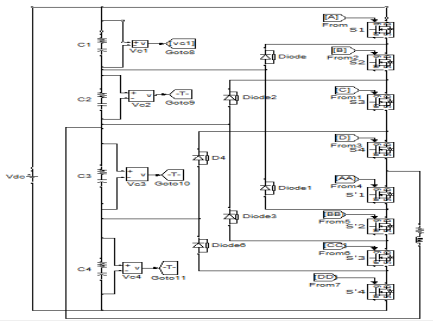

Figure 1: five -level diode clamped inverter

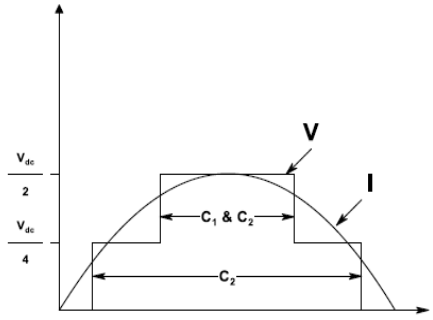

Figure 2 :DC capacitor voltage unbalancing [1]

2.1 Switching technique for multilevel inverter

The switching technique employed here is phase disposition pulse width modulation scheme.

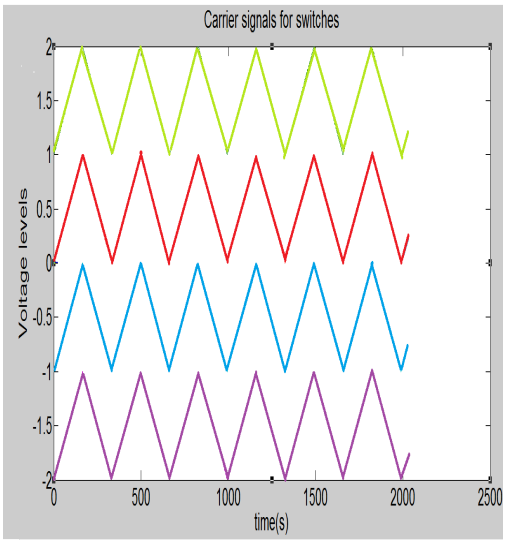

Figure 3:SPWM switching signal

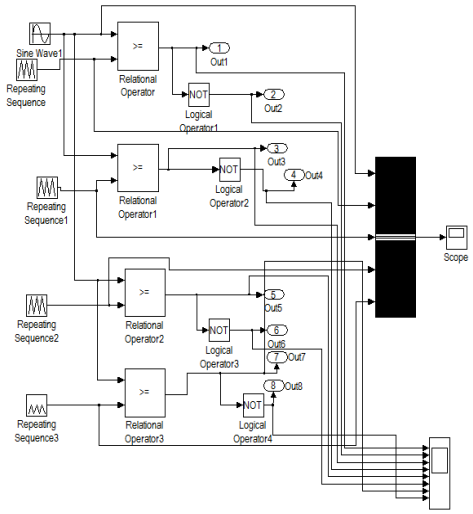

Figure 4:switching control operation

Here as shown in fig.4 the four triangular carrier signal waves are used which are all having same frequency, same amplitude and are equally displaced from each other but the only difference is change in the dc offset so as to occupy different levels. This carrier waves are then compared with the sinusoidal reference signals and based on this the switches are turned on accordingly. The other two switching scheme available are phase-opposition disposition pulse width modulation where are the two carrier wanes are in phase with each other and the other two are in opposition to first two carrier and alternate phase-opposition disposition pulse width modulation where carrier waves are alternately phase opposed to each other [1]. It is found that employing pdpwm technique reduces the THD level to 20.73% for modulation index of 0.9.For reducing the THD LC filter is being employed.

3 LC filter design

It has been determined that the output voltage and current of inverter consist of large harmonic components as a result of switching signals. By choosing a higher frequency for the inverter the higher harmonics could be filtered out more easily.LC filter is widely used for filtering out the harmonics in inverter output [5].

The value of inductor L is being calculated using the following equation:

$$L=V_p/2*2.44*f_s*i_{ripple,peak} \quad (1)$$

Where f_s is the inverter switching freqency and V_p is the rms phase voltage.The value of the inductor is selected such that the value of inductor current ripple is limited to 15%.

Similarily the value of C is being calculated using the following equation:

$$C=1/(2*\pi*f_0)^2*L \quad (2)$$

Where f_o is the cutoff frequency,this value of cutoff frequency is $1/6^{th}$ of the fundamental freqency.This LC filter is thus employed at the load side so that a filtered output provides a smooth operation for the load.By using LC filter the level of THD is reduced to 0.47%.

4 Two-level boost converter

Here in this paper the five-level diode clamped inverter inner capacitor voltage balancing is being managed by a two-level boost converter as shown in Fig5.The TLBC has advantages in reducing recovery losses of the diodes and switching losses. The conventional boost converter consists of two separate switching inductors which leads to the increase in cost of the circuit. With the introduction, of the modified boost converter in the form of two level boost-converter there is reduction in inductor ripple current because of which the size of inductor is reduced to half the size of rating requirement compared to conventional boost-converter [4].

4.1 Inner capacitor voltage balancing

The circuit for TLBC is as shown in Fig 5. The switching signal in switches S_1 and S_2 are turned on alternately here the switching signals do not overlap each other for some duration of time since they are turned alternately on and off [5]. The switching signal shown are for the duty ratio of 0.5. This TLBC operates in four different modes.

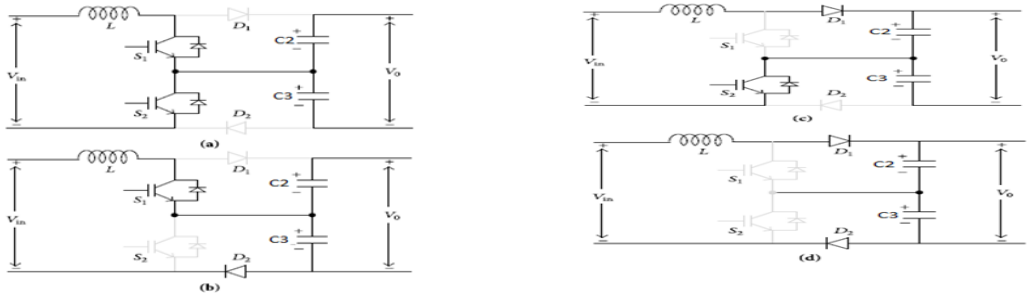

Figure 6: Modes of boost converter

In mode (a) both the switches S_1 and S_2 are on. Followed by alternate switching on and off of the switches in mode (b) and mode (c) respectively and switching of both the switches in mode 4 where the load is directly being supplied by the source. In mode (a) energy is being stored in the inductor as both S_1 and S_2 are in on condition. In mode (b) and (c) C_2 and C_3 are alternately charged to a higher level and in mode (d) load is directly supplied by the source. Capacitors C_2 and C_3 can be charged to the required voltage level by changing the duty ratio interval with the help of changing in the charging

duration. TLBC could be operated in five different algorithms [5].In this paper,one of the algorithm where time switching of S_1 and S_2 overlap each other is used.

5 Simulations and results

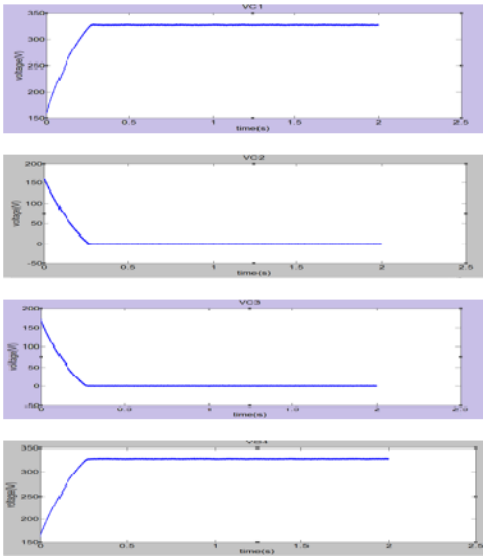

Figure 7: unbalancing in capacitor voltages

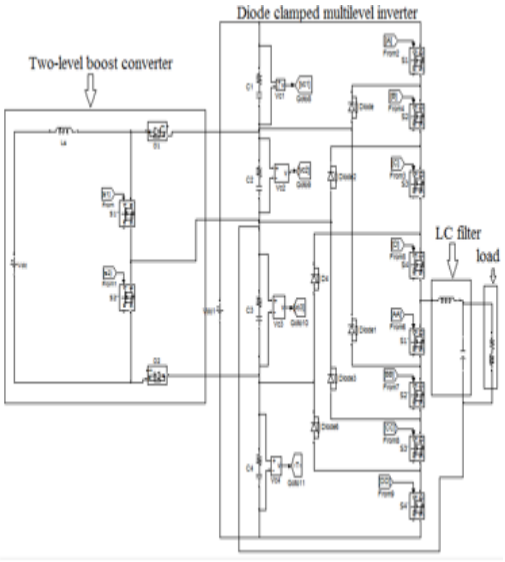

Figure8: boost converter with inverter

Parameters	Value
DC source voltage for boost converter	180V
DC source voltage for inverter	625V
DC capacitor voltage	2200microfarad
Carrier frequency in boost converter	5KHz
Carrier frequency in inverter	5.5khz

Table-1 parameters for simulation circuit

fg.7 shows the unbalancing in the capacitor voltages which is being balanced by addition of boost-converter as shown in fig. 8. This circuit is being tested for different resistive values of 50 ohms and 54ohm and inductive load of L=28.7mH and 32.7mH. as shown in fig.9

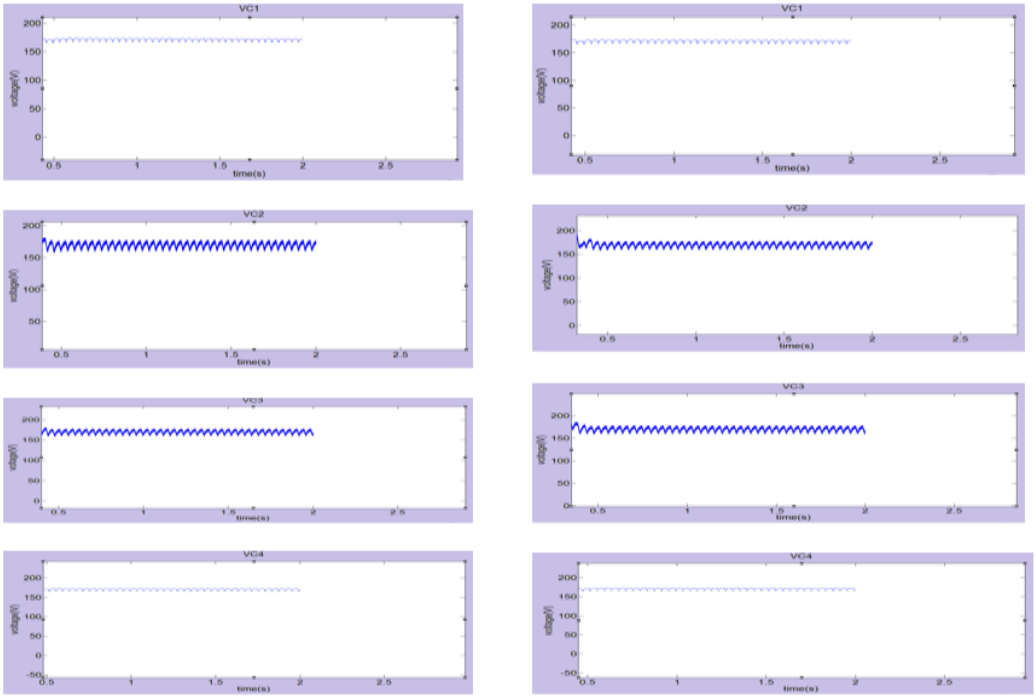

Figure9: Balancing after boost converter

6 Conclusion

The research conducted in this configuration works well for balancing of the capacitor voltages leading to the uniformity in the output voltage in terms of maintaining the required output voltage levels and increase in the life of dc link capacitor by appropriate usage of all the capacitors voltage levels. The circuitry could thus be employed for different loading conditions

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